

# WASP 13 CS Whiskey Lake-U

2019-01  
REV : A00

*DY : None Installed*  
*UMA: UMA only installed*  
*OPS: DIS only installed*

<Core Design>



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Title

**Cover Page**

Size  
A4

Document Number

**WASP 13" WHL-U**

Rev

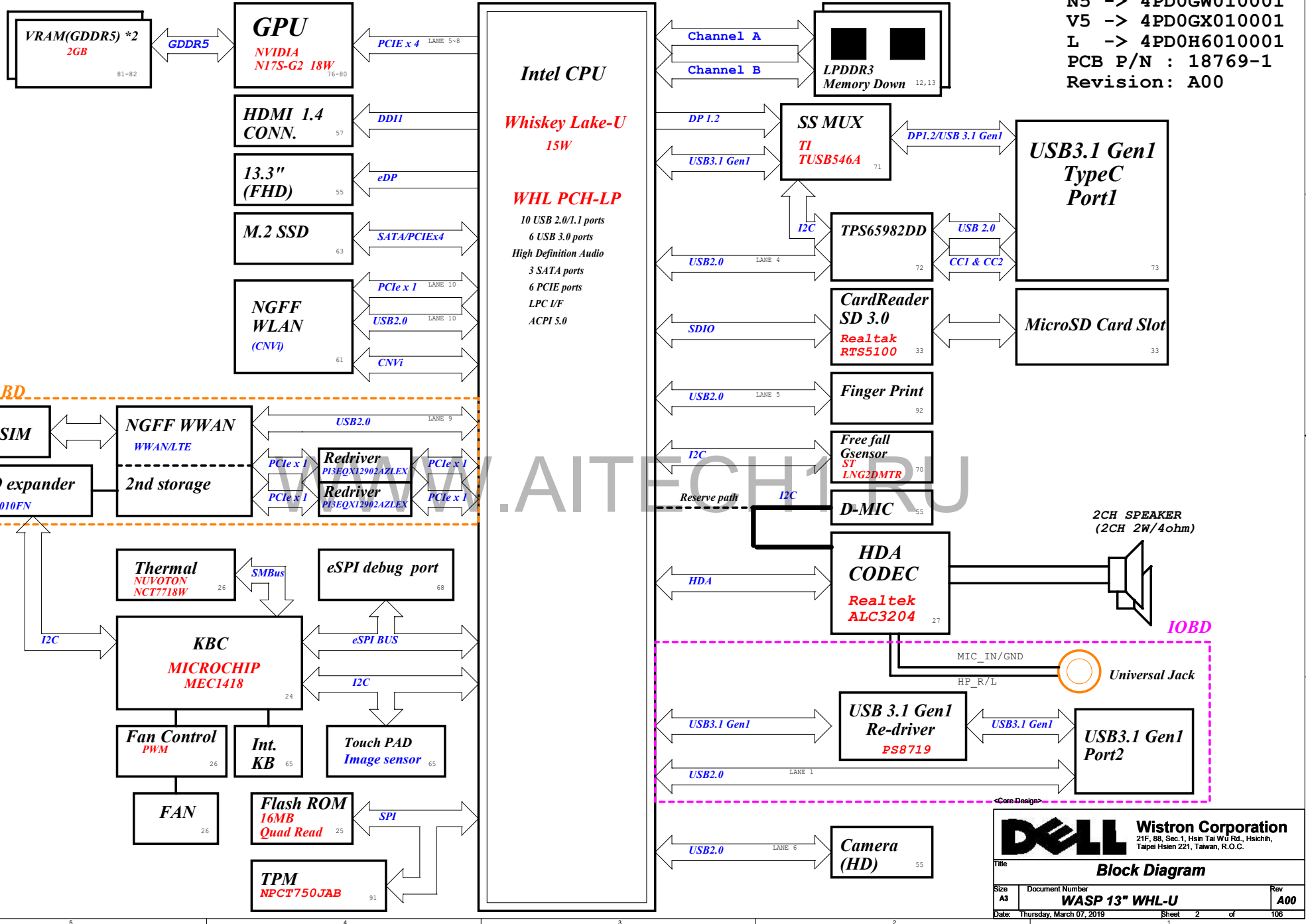
**A00**

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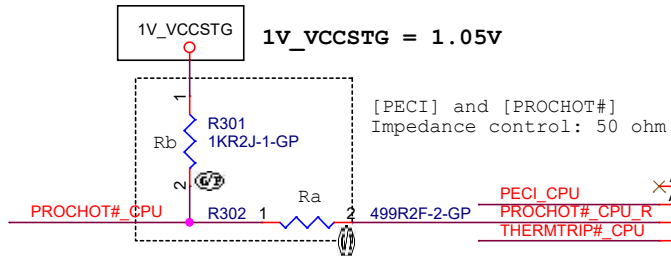
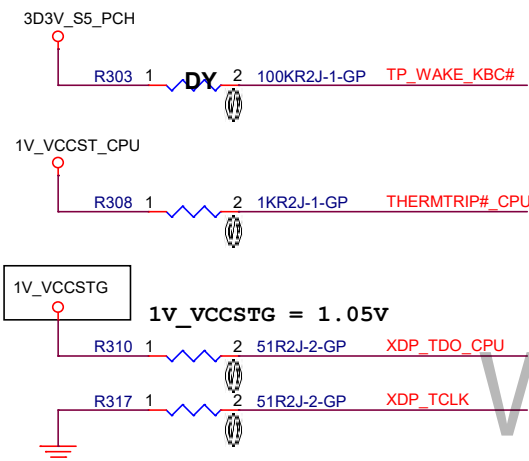
# WASP 13" CPU 15W + GPU 18W Block Diagram

Project code :  
 N5 -> 4PD0GW010001  
 V5 -> 4PD0GX010001  
 L -> 4PD0H6010001  
 PCB P/N : 18769-1  
 Revision: A00



# Main Func = CPU

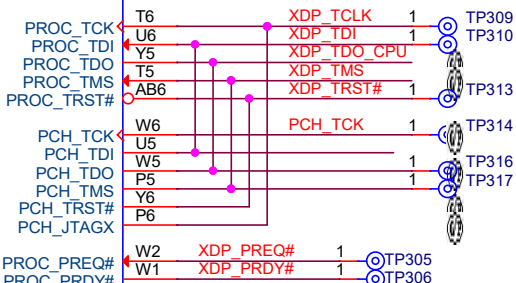
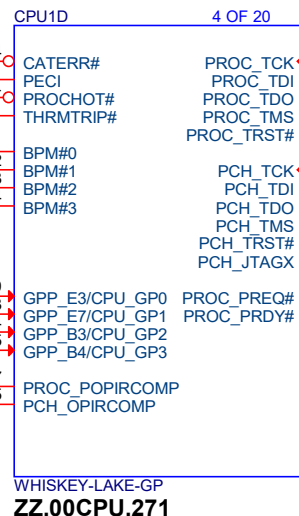
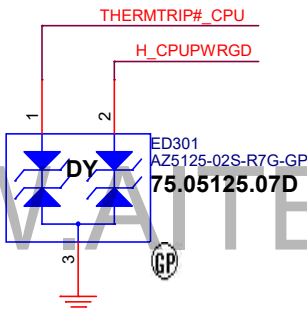
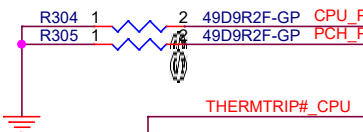
24 PECI\_CPU <<>>  
 24,44,46 PROCHOT#\_CPU <<>>  
 55 TOUCH\_PANEL\_INTR# <<<<  
 24,65 TP\_WAKE\_KBC# >>>>  
 55 TOUCH\_PANEL\_PD# <<<<  
 17 H\_CPUPWRGD >>>>



499R2F-2-GP  
 499R2F-2-GP  
 499R2F-2-GP

TP307 1 BPM\_N0 U1  
 TP308 1 BPM\_N1 U2  
 TP302 1 BPM\_CPU\_N2 U3  
 TP303 1 BPM\_CPU\_N3 U4

TP304 1 GPP\_E3/CPU\_GP0 CE9  
 TOUCH\_PANEL\_INTR# CN3  
 TP\_WAKE\_KBC# CB34  
 TOUCH\_PANEL\_PD# CC35



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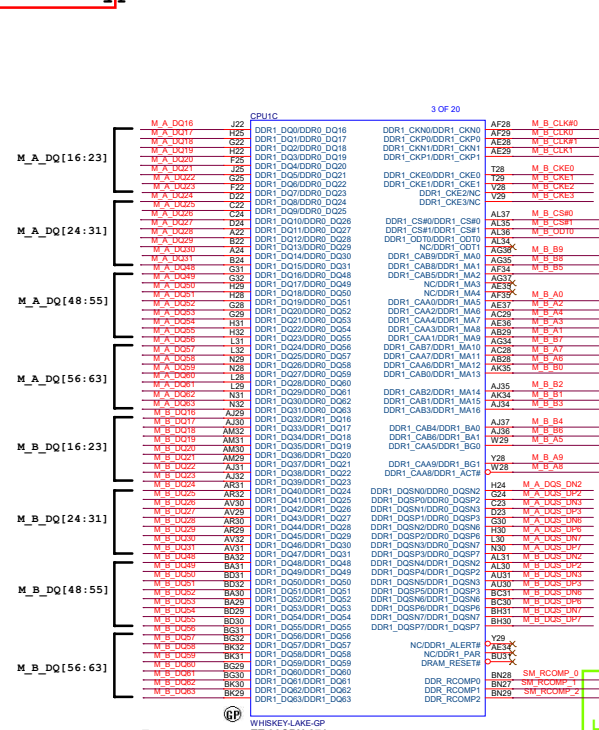
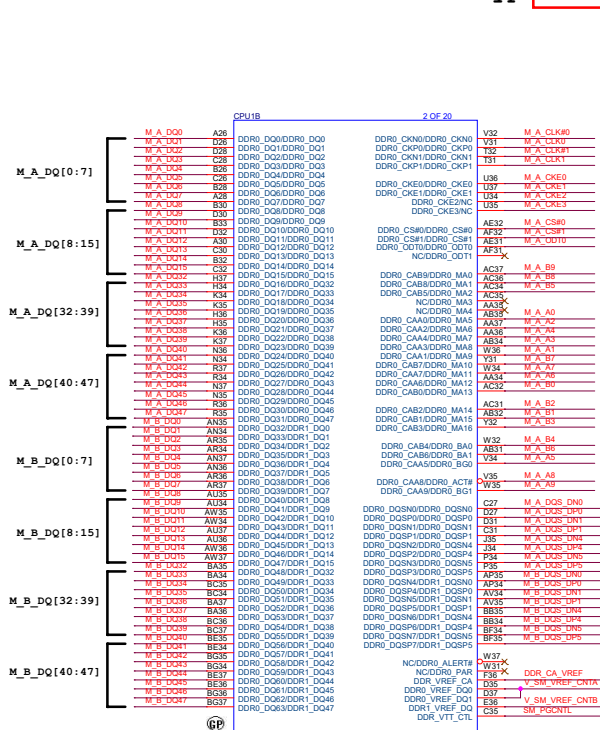
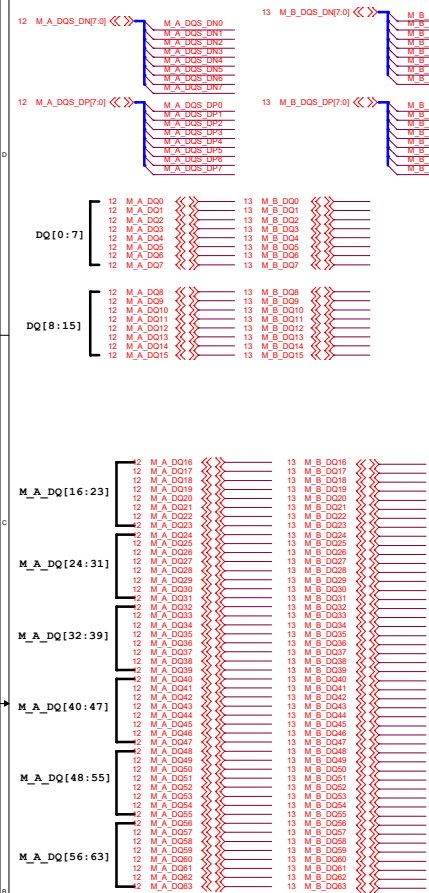
Title: **CPU (THML/JTAG)**

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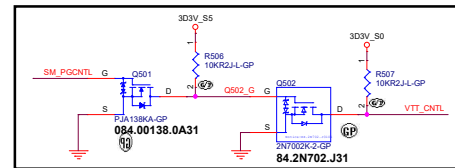
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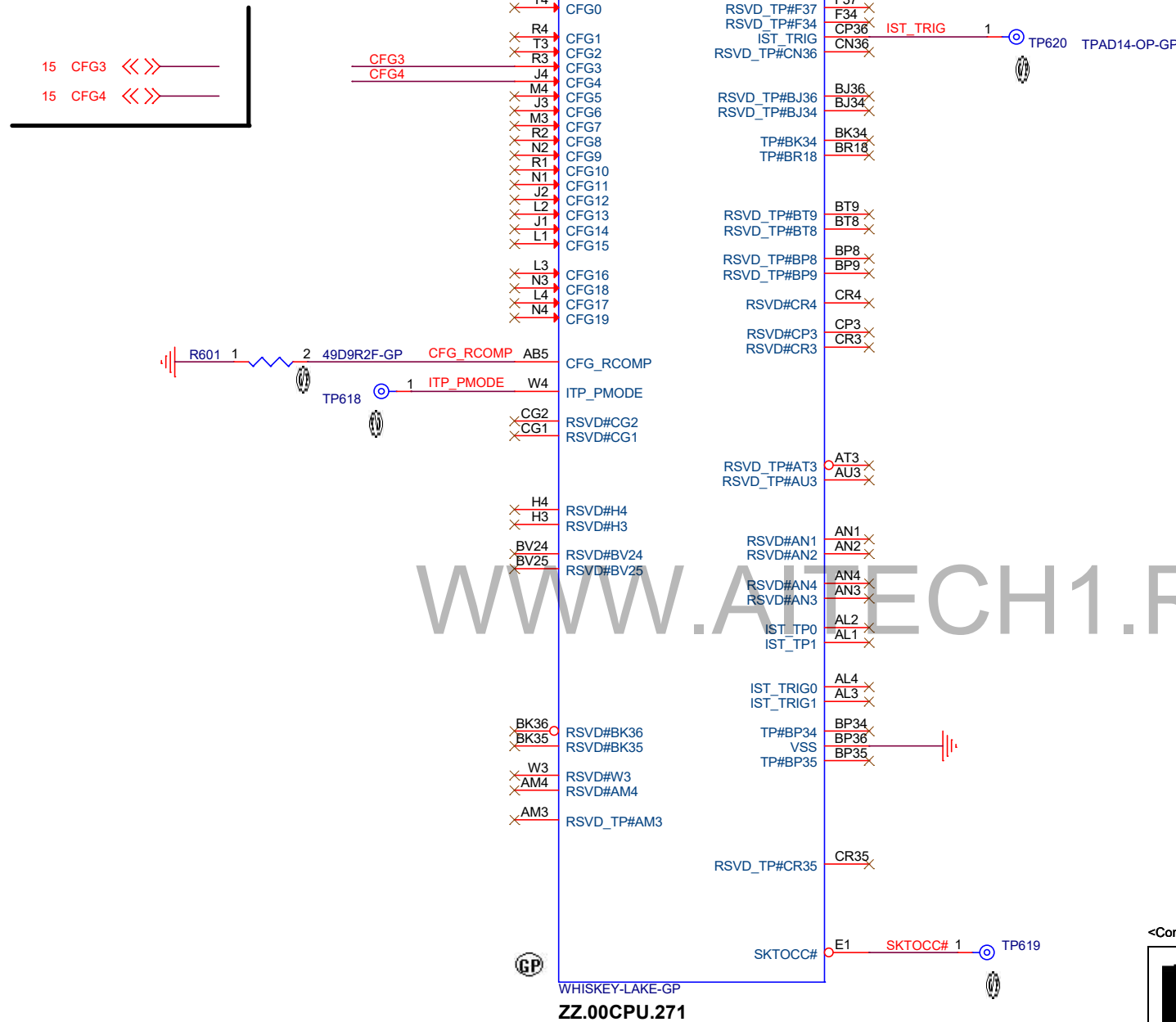
Layout Note:

Design Guideline:  
SM\_RCMP comp routing length less than 500 mils.

&lt;Core Design&gt;

**DELL** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,  
Taipei Hsin 321, Taiwan, R.O.C.File: **CPU (DDR)**  
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Main Func = CPU



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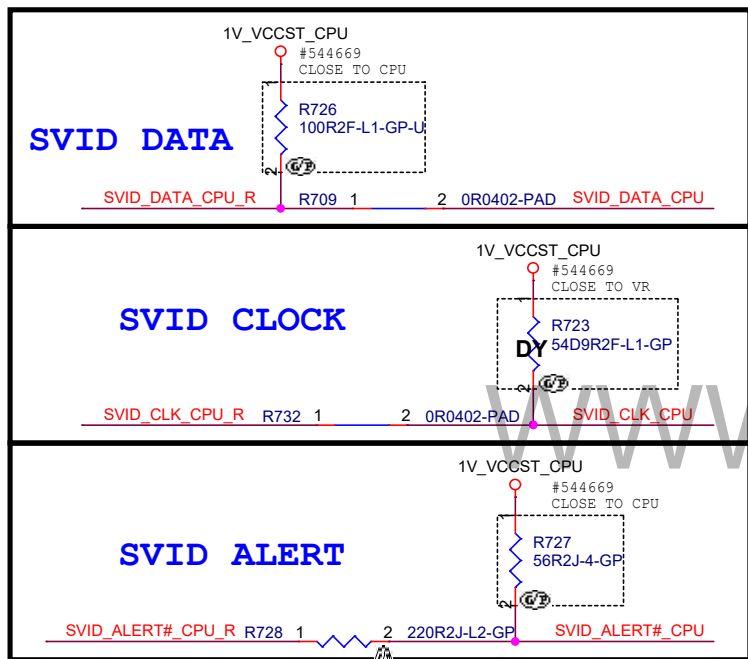
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Size: A4	Document Number: <b>WASP 13" WHL-U</b>	Rev: <b>A00</b>
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# Main Func = CPU

46 VCCCORE\_SENSE <<<<  
46 VSSCORE\_SENSE <<<<  
46 SVID\_DATA\_CPU <<>>  
46 SVID\_CLK\_CPU <<<<  
46 SVID\_ALERT#\_CPU <<<<

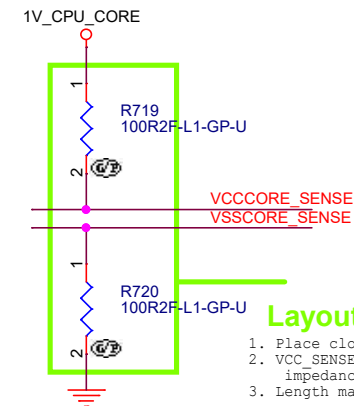
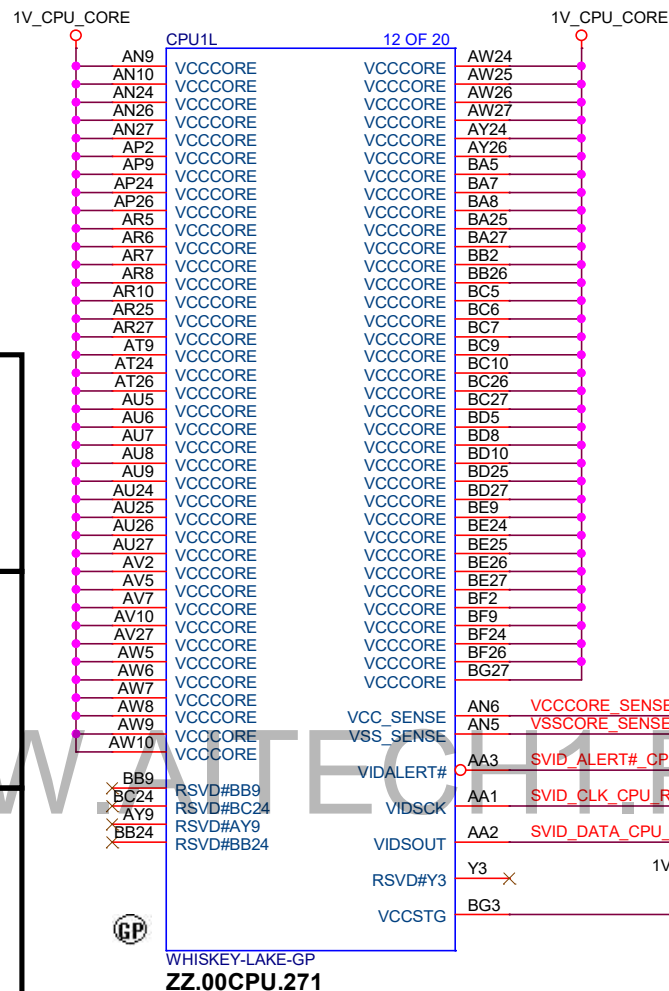


## SVID\_543016:

Layout Note:  
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).  
Route the Alert signal between the Clock and the Data signals.

Table 10-10.SVID Bus Routing Guidelines

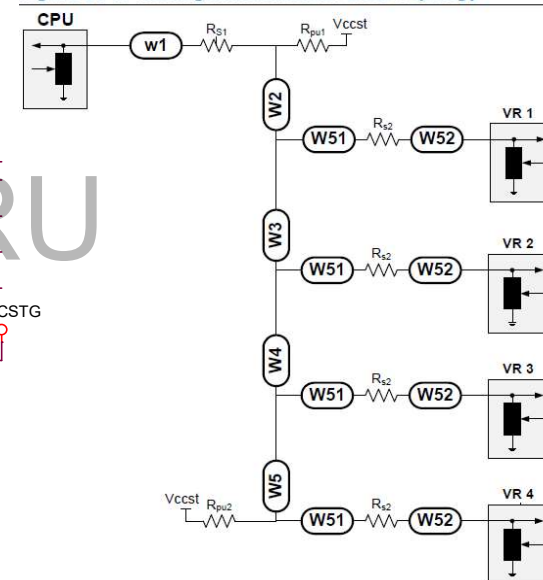
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>pu1</sub> [Ω]	R <sub>pu2</sub> [Ω]	R <sub>s1</sub> [Ω]	R <sub>s2</sub> [Ω]	VCC <sub>cr</sub> [V]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	
VIDALERT #							56	Empty	220	0	1.0



## Layout Note:

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 Ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology



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**CPU (VCORE/VID)**

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**(Reserved)**

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A4

Document Number

**WASP 13" WHL-U**

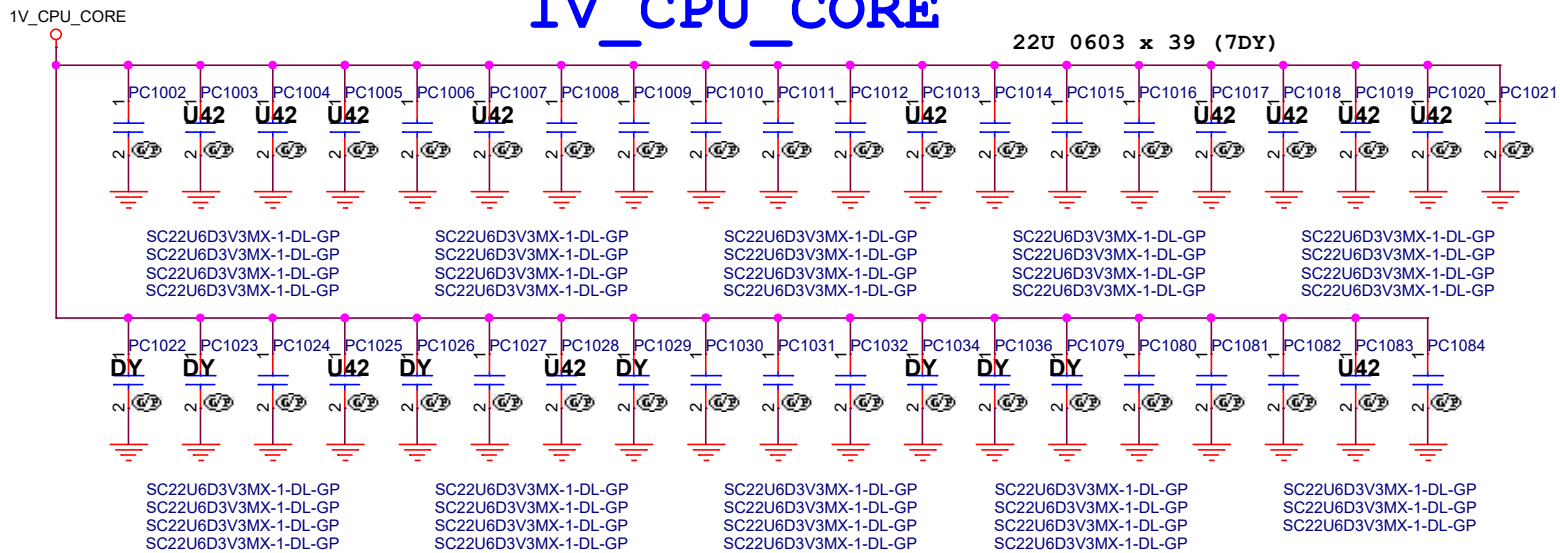
Rev  
**A00**

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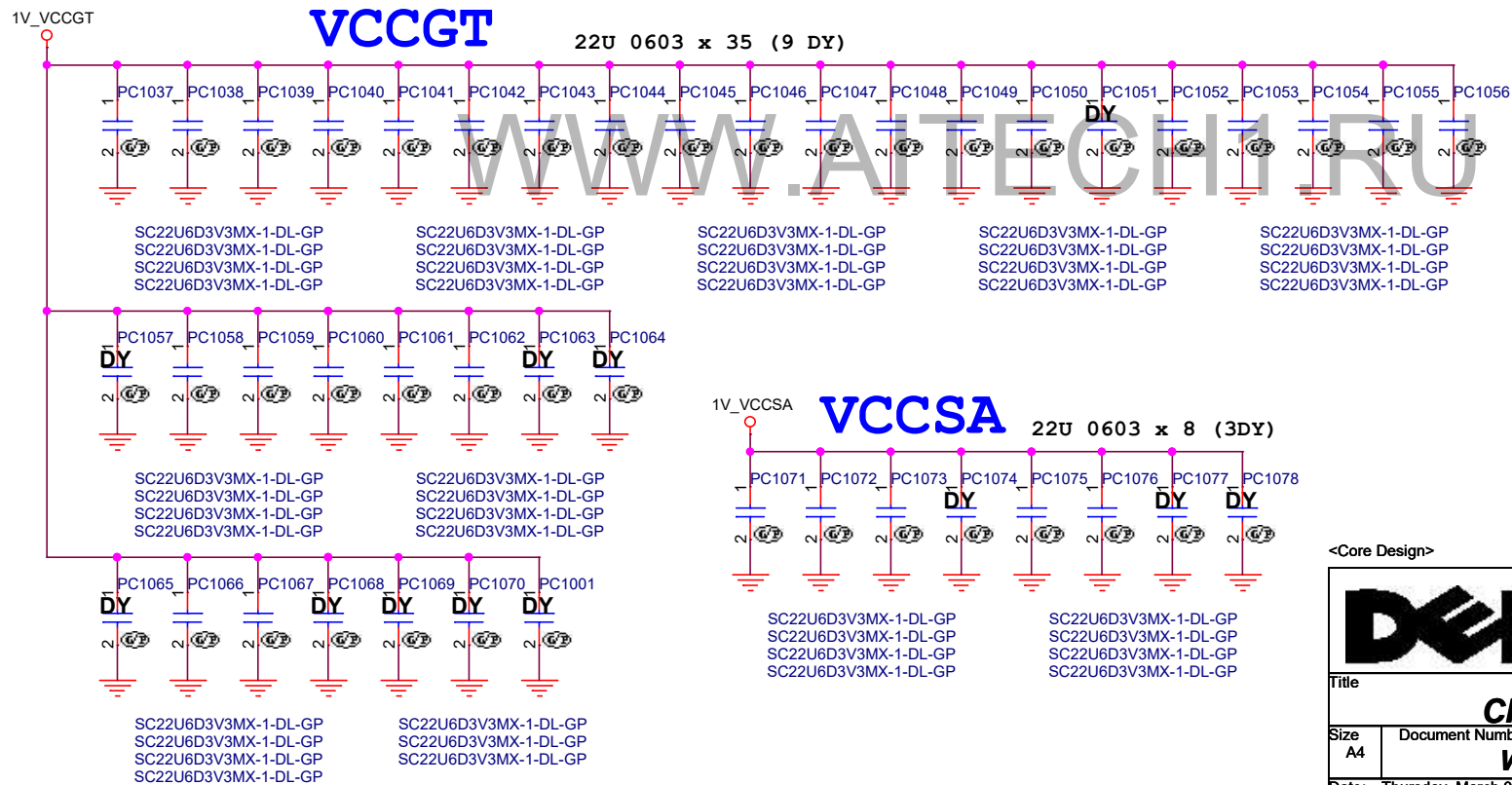
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**Main Func = CPU**

# 1V CPU CORE



# VCCGT



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### CPU (Power CAP1)

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Document Number

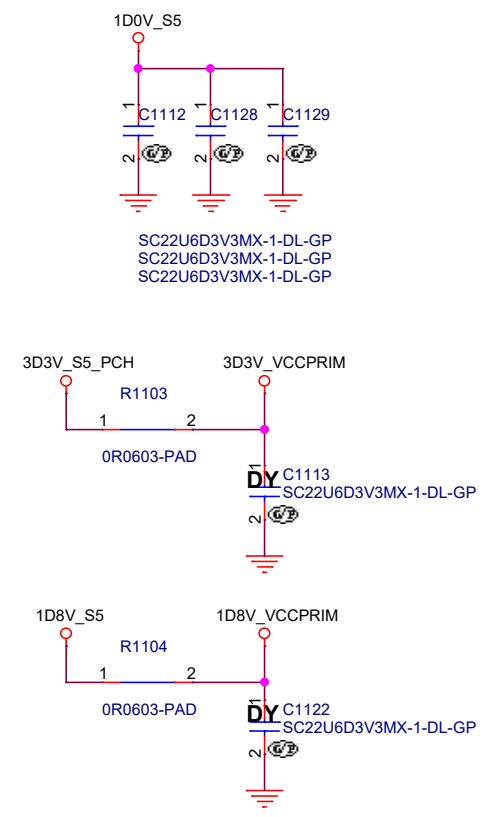
**WASP 13" WHL-U**Rev  
**A00**

Date: Thursday, March 07, 2019

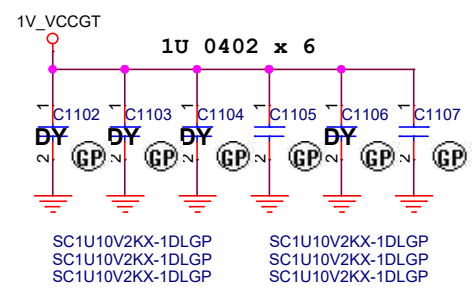
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Main Func = CPU

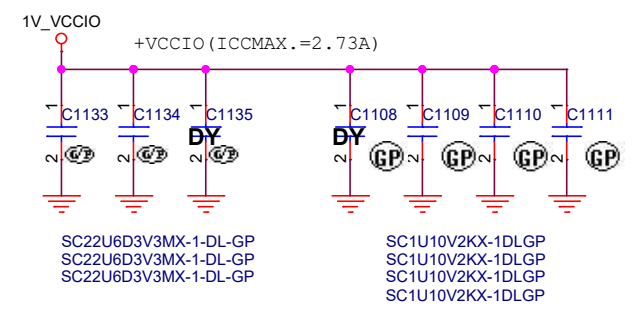
PCH DERIVED RAILS



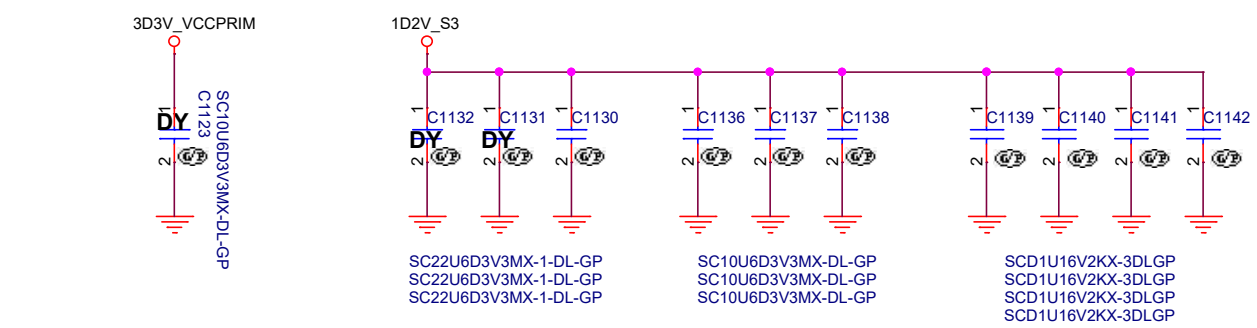
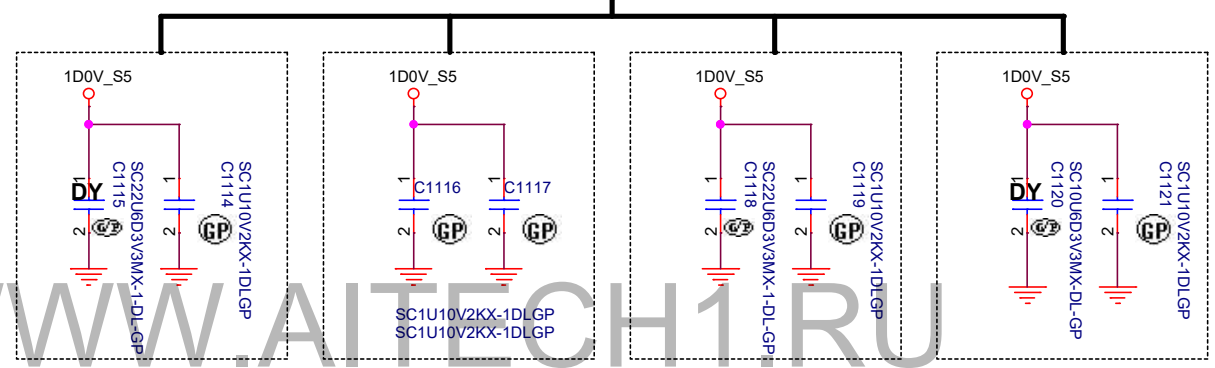
UNSLICED GT



VCCIO



+VCCMPHYGTAON\_1P0 (ICCMAX.=2.12A)



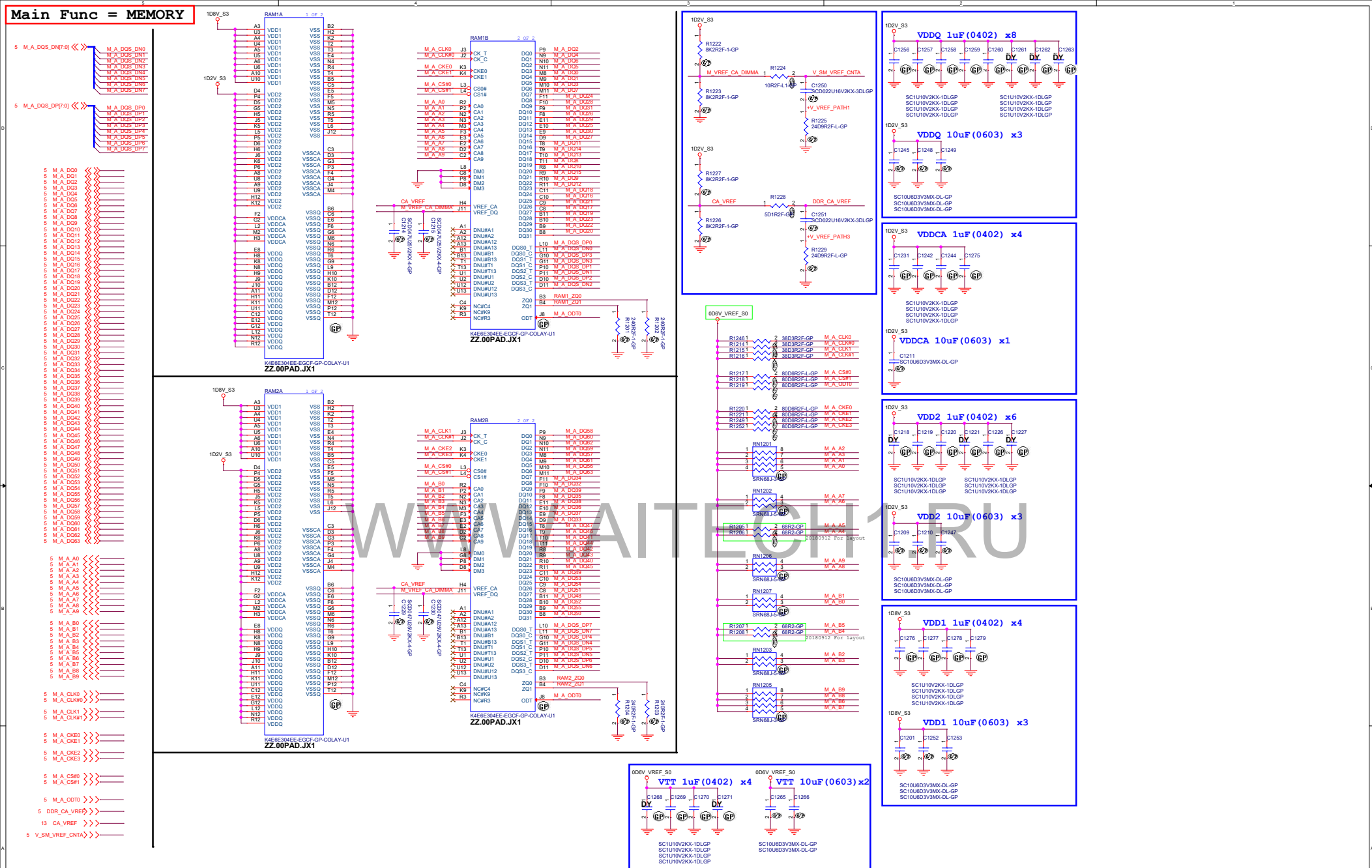
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Title		
CPU (Power CAP2)		
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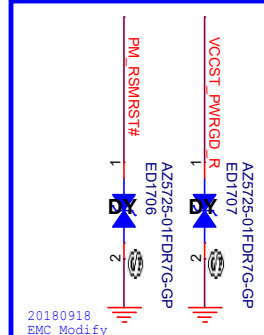
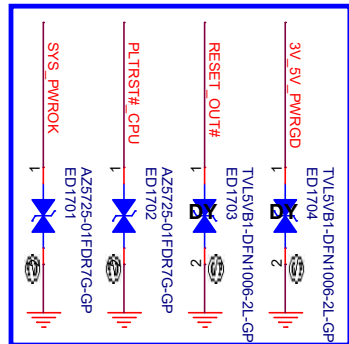




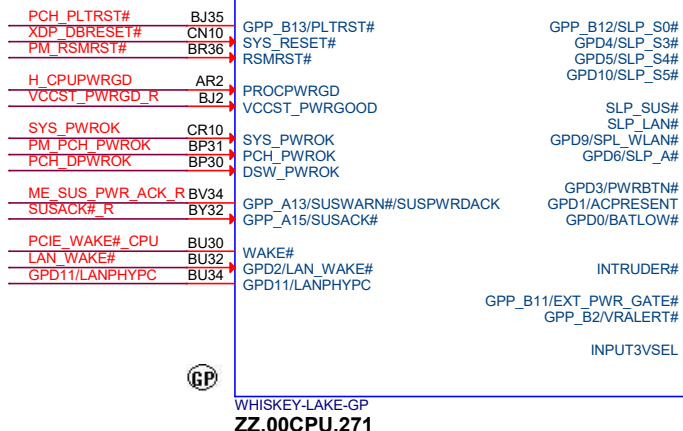
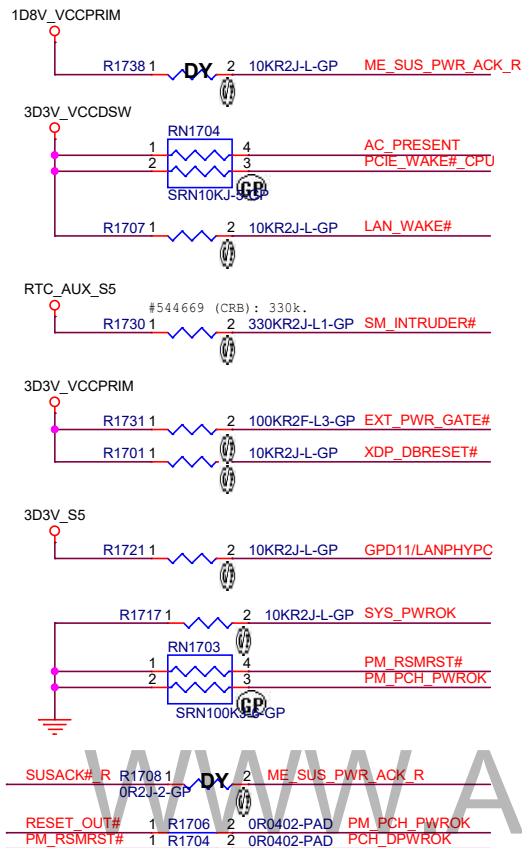
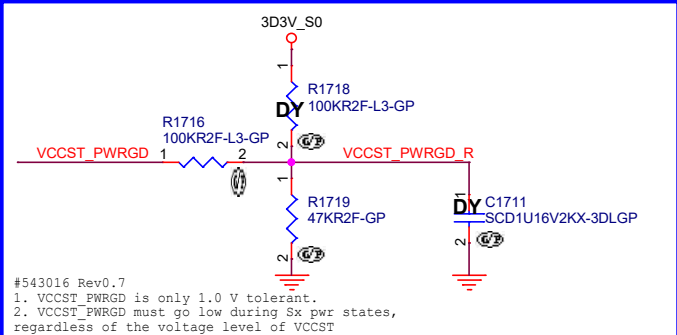
# Main Func = PCH

24 SYS\_PWROK >>>  
 24,26 RESET\_OUT# >>>  
 24,40,46 VCCST\_PWRGD >>>  
 24,64 PCH\_RSMRST# >>>  
 25,45 3V\_5V\_PWRGD >>>  
 40,91 PM\_SLP\_S0# <<<  
 40 PM\_SLP\_S3# <<<  
 40,51,92 PM\_SLP\_S4# <<<  
 24 SIO\_PWRBTN# >>>  
 44 AC\_IN# >>>  
 15 INPUT3VSEL >>>  
 61,63,66,76,91 PLTRST#\_CPU <<<  
 3 H\_CPUUPWRGD <<<

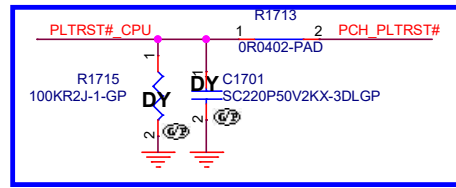
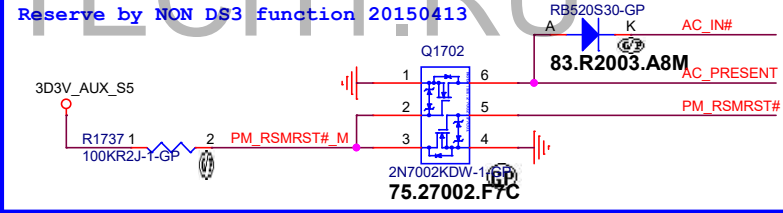
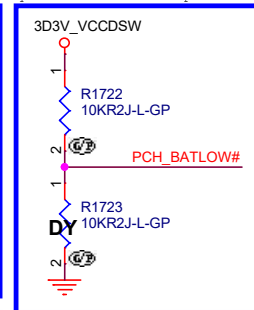
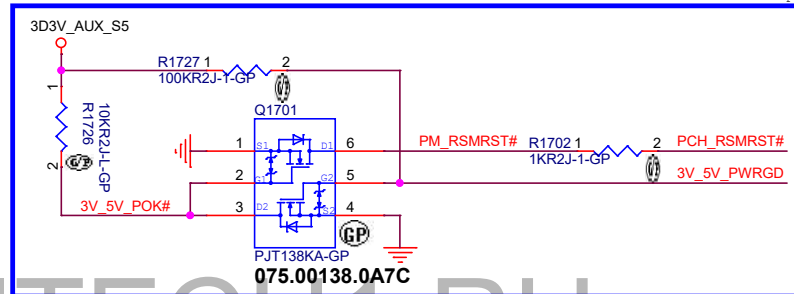
20180905  
 EMC add



20180918  
 EMC Modify



BATLOW#:  
 Pull-up required even if not implemented

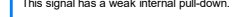
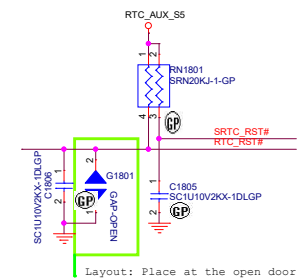


(PDG#543016)  
 WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

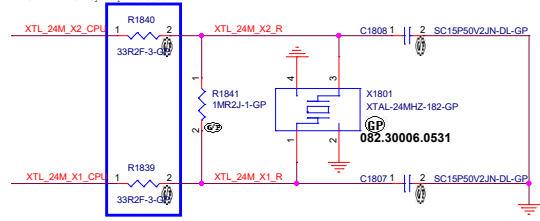
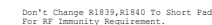
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Title <b>CPU (POWER MANAGEMENT)</b>			Rev <b>A00</b>
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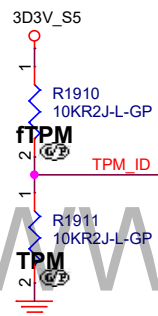
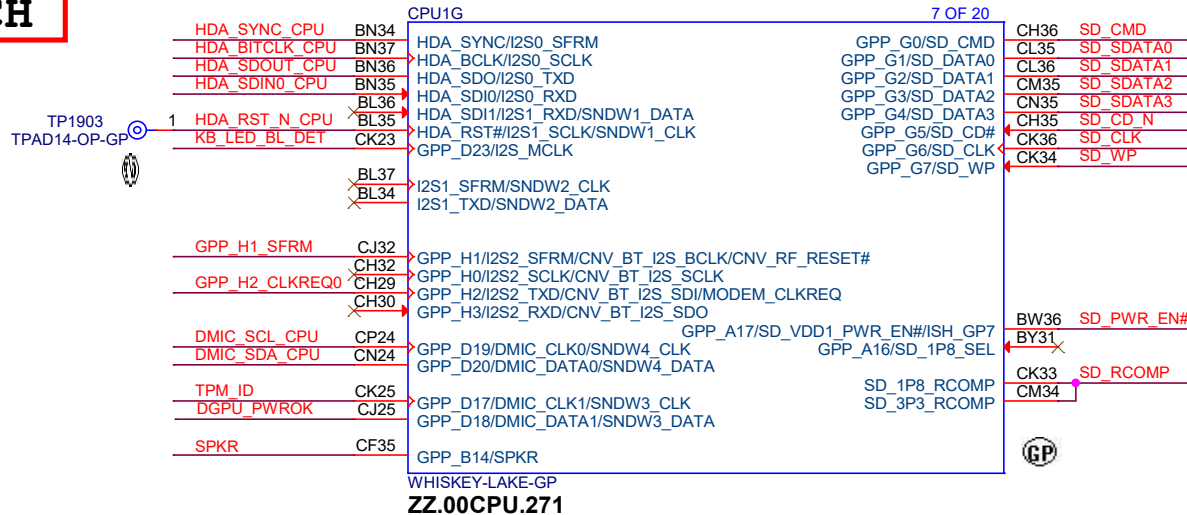
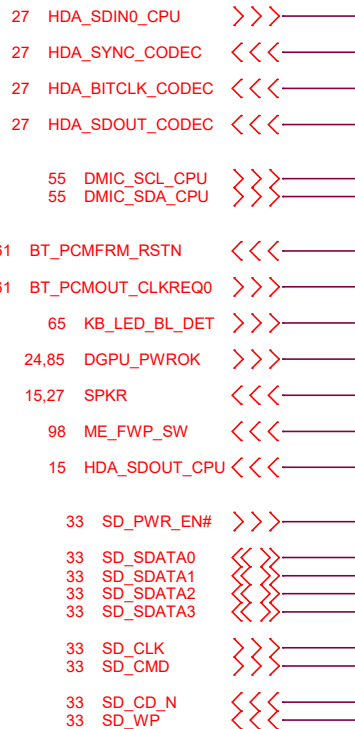


Signal	Usage	When Sampled	Comment
			<p>This signal has a weak internal Pull-up.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device3, Function), offset BCh bit 6).</p>
			<p style="text-align: center;"><b>Bit 6</b></p> <p style="text-align: center;"><b>Boot BIOS Destination</b></p> <p style="text-align: center;"><b>SPI (Default)</b></p> <hr/> <p style="text-align: center;">0                      1                      LPC</p>
<b>GPSTL_MOSI / GPP_B22</b>	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWRGD	<p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is disabled after PLTRST# de-asserts.</li> <li>If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid destination in order to boot.</li> <li>Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ICH or Integrated GME IAN.</li> <li>This signal is in the primary well.</li> </ol>
			<p>This signal has a weak internal Pull-up.</p> <p>0 = <b>eSPI</b> is selected for EC. (Default)</p> <p>1 = <b>eSPI</b> is selected for EC.</p>
<b>SMIOALERT# / GPP_CS</b>	eSPI or LPC	Rising edge of RSMRST#	<p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The internal Pull-down is disabled after RSMRST# de-asserts.</li> <li>This signal is in the primary well.</li> </ol>



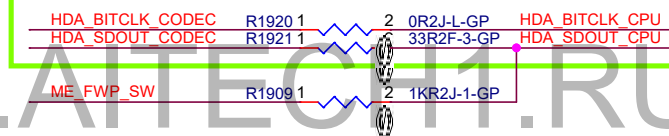


# Main Func = PCH



## Layout Note:

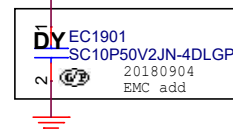
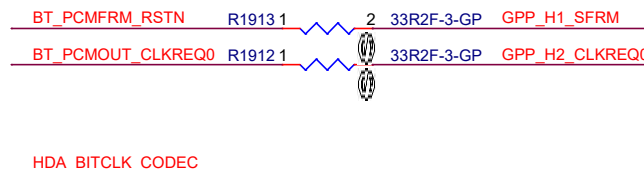
R1920 & R1921 need to close for merge prepare



## Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



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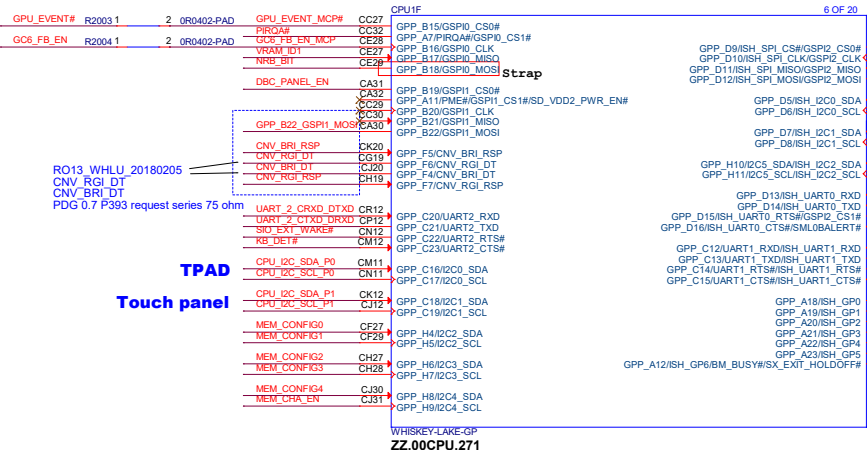
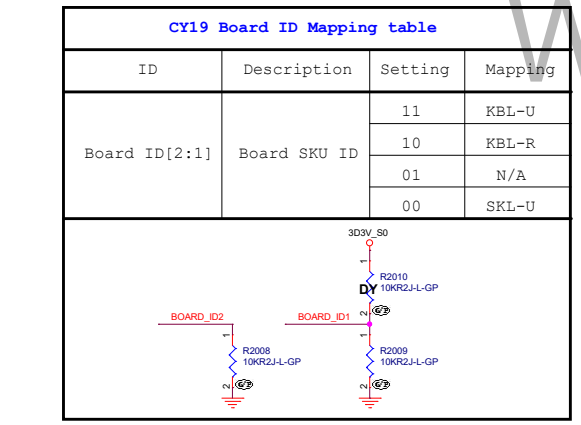
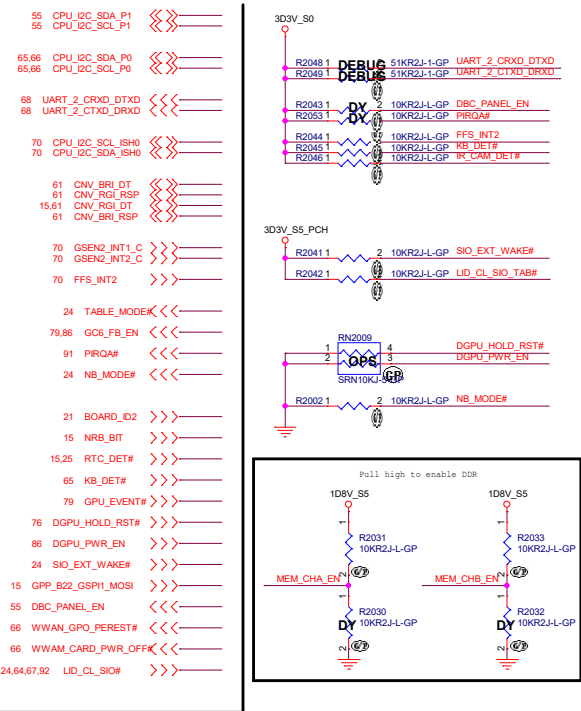
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Title: **CPU (HDA/I2S/SD/DMIC)**

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Main Func = PCH



**CY19 MEM\_CONFIG Mapping table**

ID	Description	Setting	Mapping
MEM_CONFIG[4:3]	On-board memory configuration for chip vendor	11	DIMM Design
		10	Micron
		01	Hynix
		00	Samsung
MEM_CONFIG[2:1]	On-board memory configuration for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	SDP/DDP Configuration	1	SDP
		0	DDP

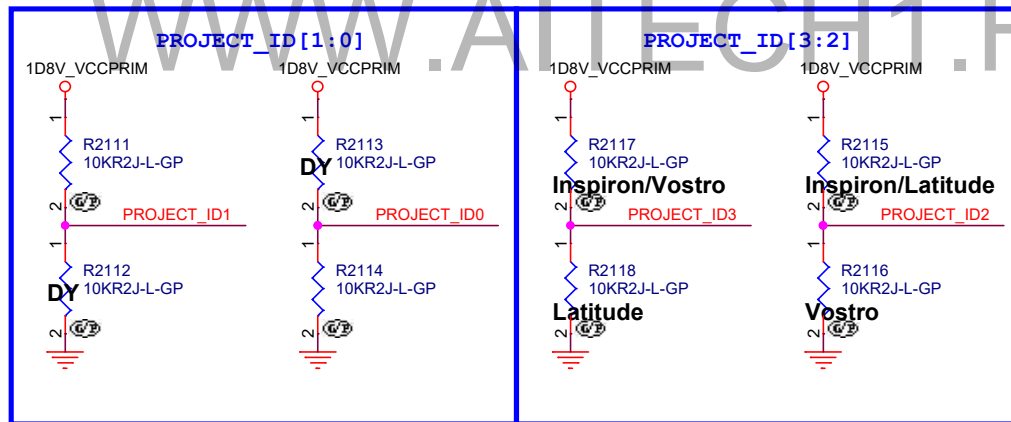
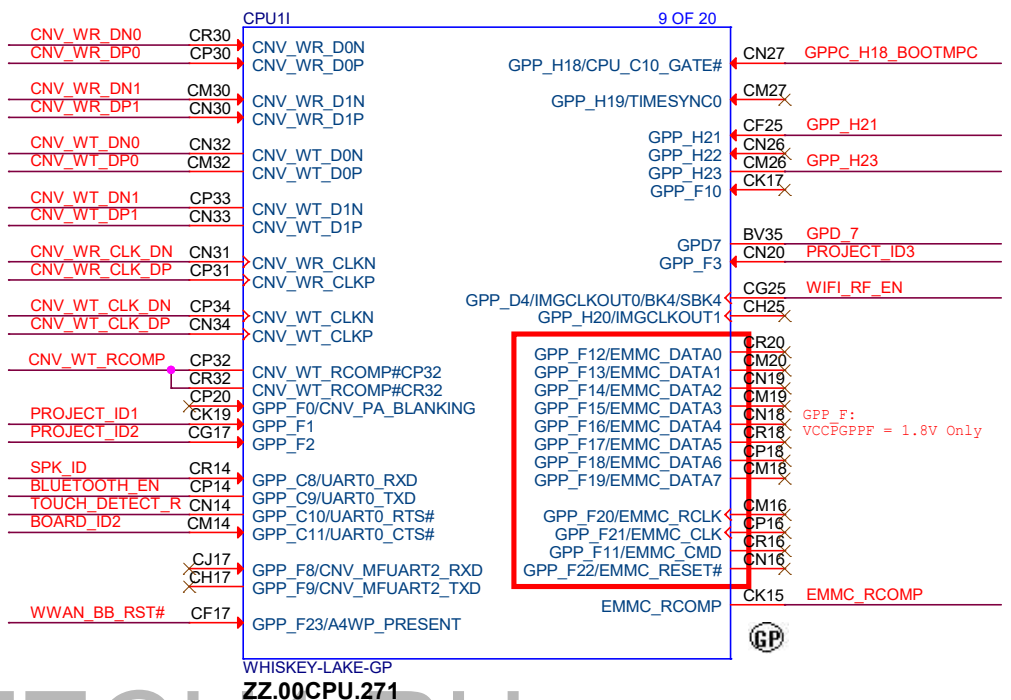
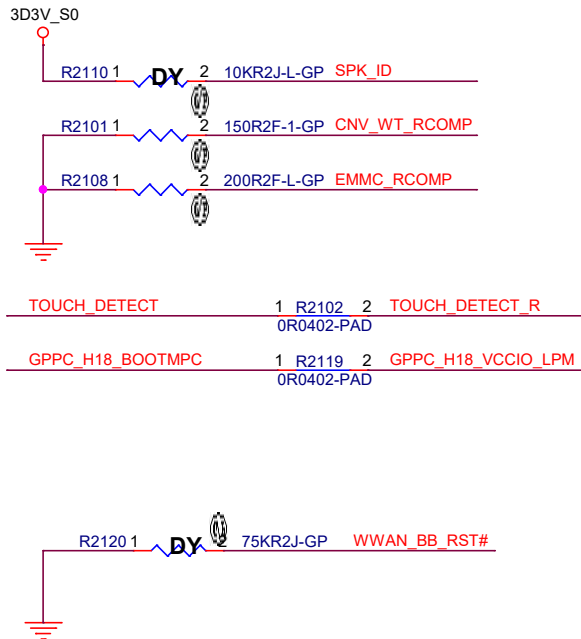
**CY19 VRAM ID Mapping table**

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM



# Main Func = PCH

15 GPD\_7 >>>  
15 GPP\_H21 >>>  
15 GPP\_H23 >>>  
18 PROJECT\_ID0 <<<  
20 BOARD\_ID2 <<<  
40 GPPC\_H18\_VCCIO\_LPM <<<  
55 TOUCH\_DETECT >>>  
21,61 CNV\_WR\_CLK\_DP >>>  
21,61 CNV\_WR\_CLK\_DN <<<  
21,61 CNV\_WR\_CLK\_DP <<<  
21,61 CNV\_WR\_CLK\_DN <<<  
61 CNV\_WR\_DP0 <<<  
61 CNV\_WR\_DN0 <<<  
61 CNV\_WR\_DP1 <<<  
61 CNV\_WR\_DN1 <<<  
61 WIFI\_RF\_EN <<<  
61 BLUETOOTH\_EN <<<  
61 CNV\_WT\_CLK\_DP >>>  
61 CNV\_WT\_CLK\_DN >>>  
61 CNV\_WT\_DP0 >>>  
61 CNV\_WT\_DN0 >>>  
61 CNV\_WT\_DP1 >>>  
61 CNV\_WT\_DN1 >>>  
66 WWAN\_BB\_RST# <<>>



ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude Reseved
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Sereis
		01	7000 Sereis
		00	N/A

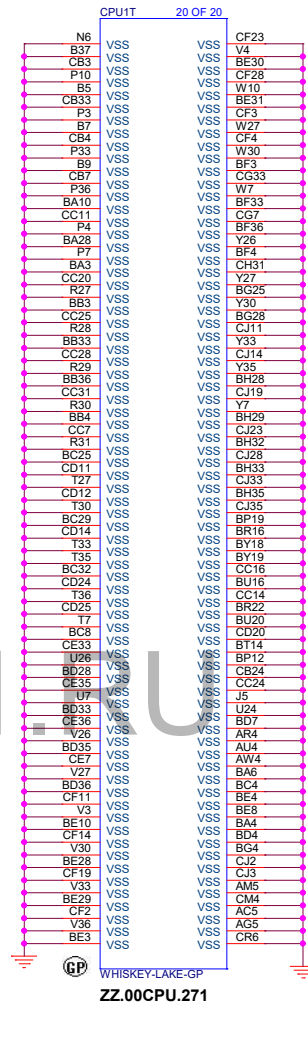
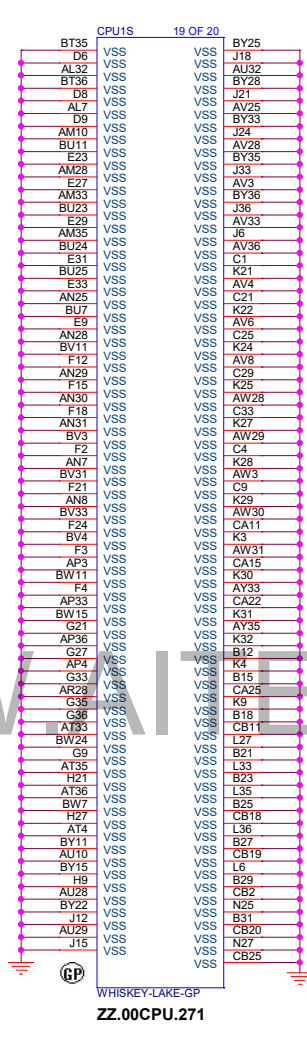
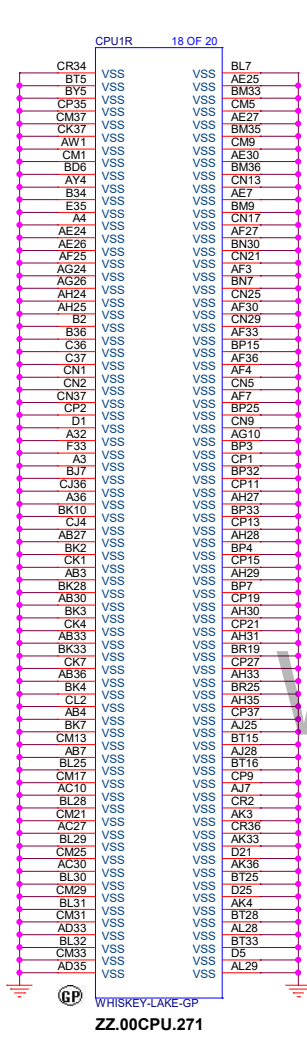
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Title		
CPU (POWER1)		
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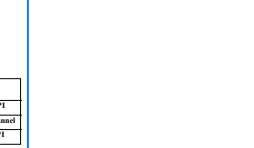
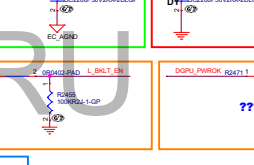
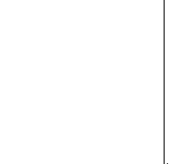
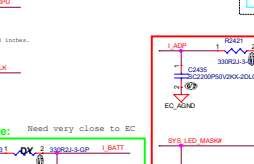
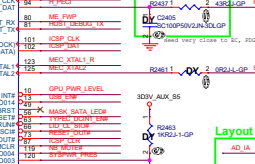
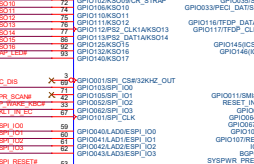
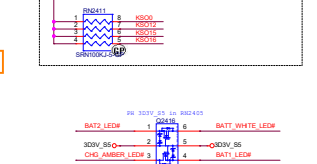
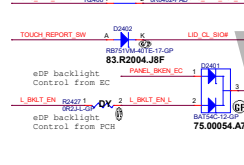
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**CPU (VSS)**

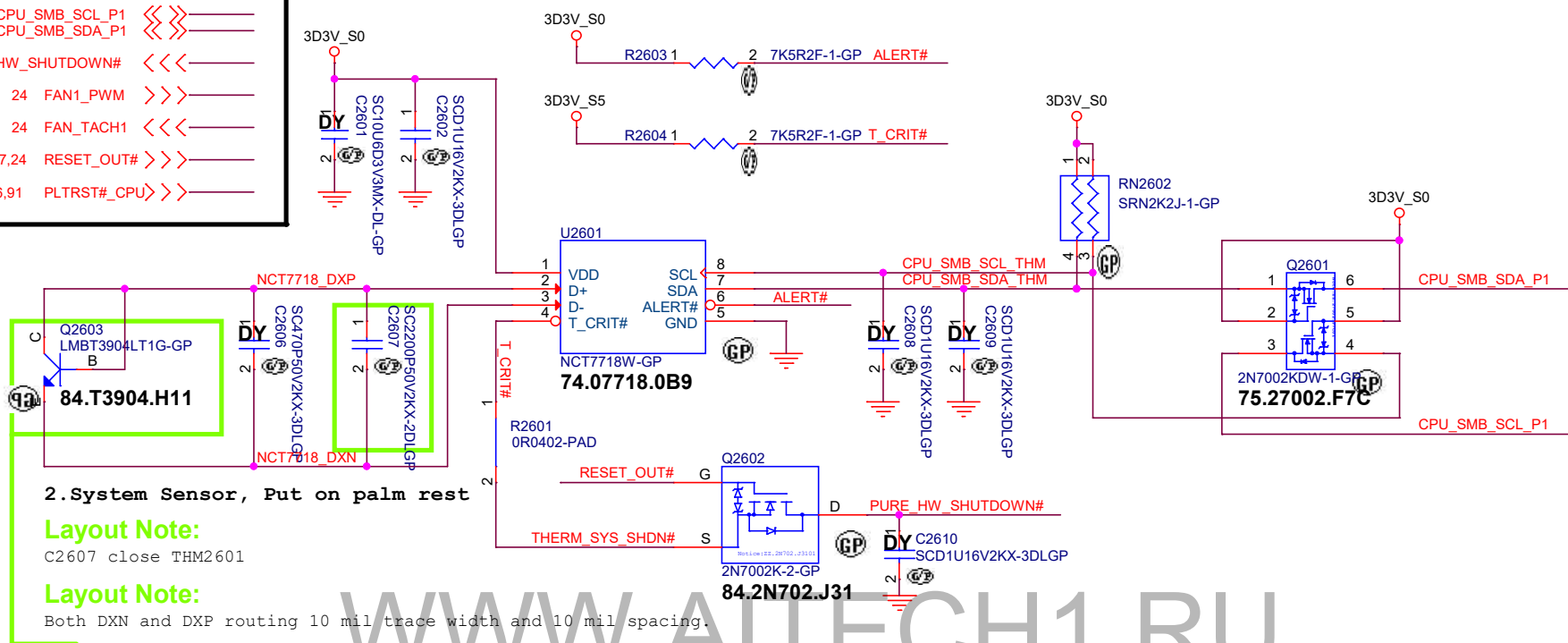
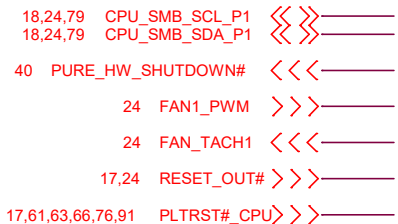
Size A3 Document Number **WASP 13" WHL-U** Rev **A00**

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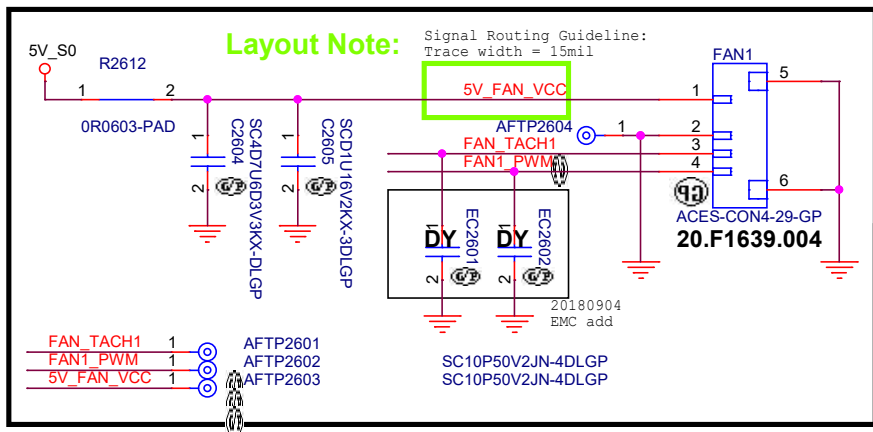
[illegible]



## Main Func = Thermal Sensor



## PWM FAN1



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

**KBC T8**

## <Core Design>



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**THERMAL NCT7718W/Fan**Size  
A4

Document Number

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## WASP 13" WHL-U

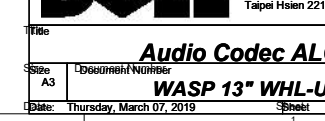
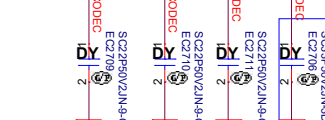
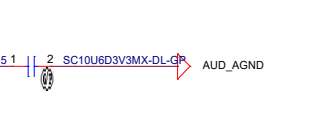
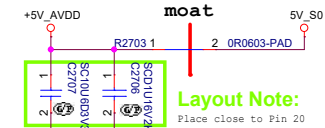
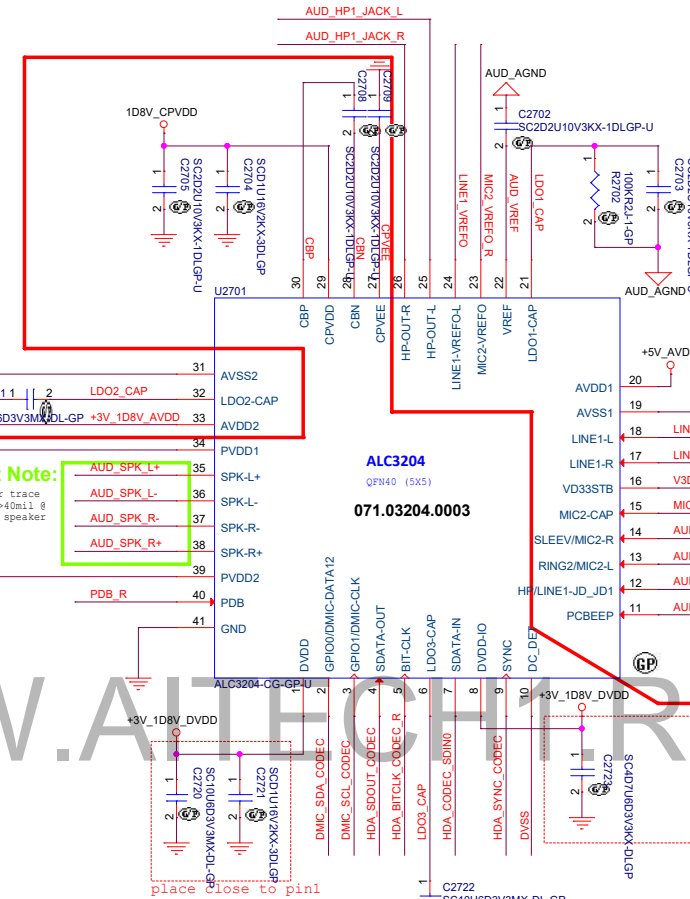
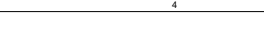
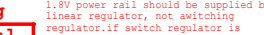
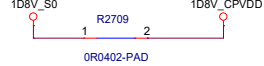
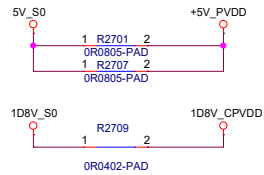
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Trev



# Audio Codec Chip ALC3204



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Size  
A4

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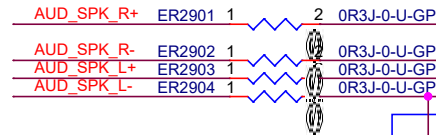
# Main Func = Audio

## Speaker

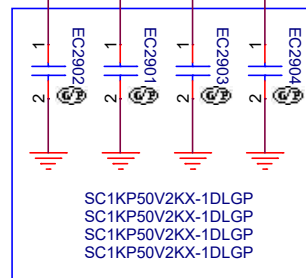
### Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

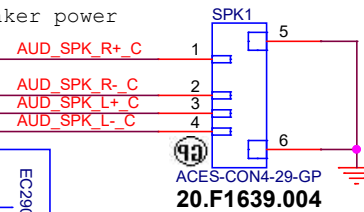
27 AUD\_SPK\_R+ <<<  
27 AUD\_SPK\_R- <<<  
27 AUD\_SPK\_L- <<<  
27 AUD\_SPK\_L+ <<<



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R+
Pin4	SPK_R-



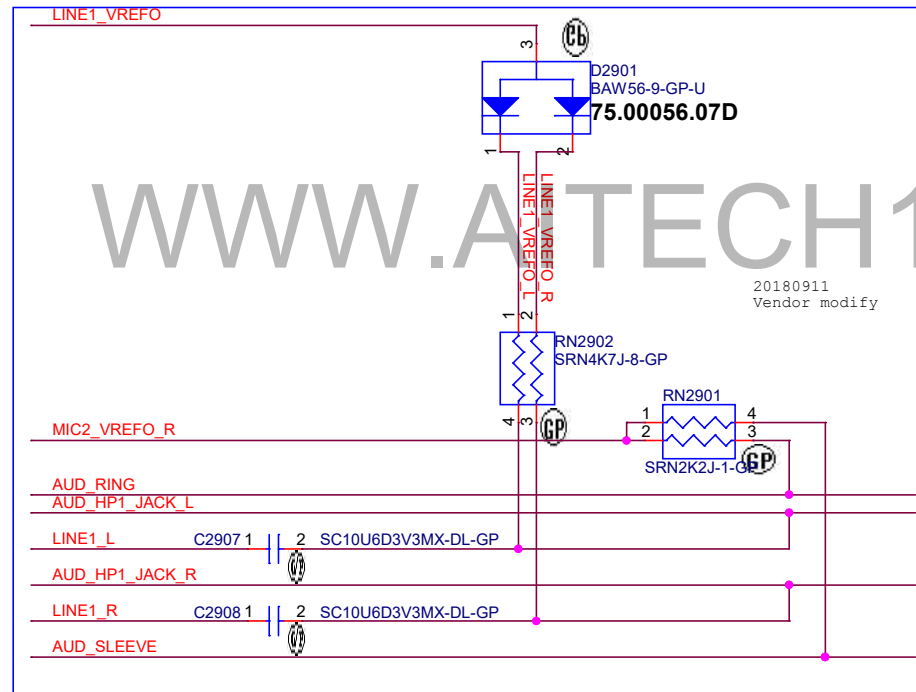
20180911  
Vendor modify



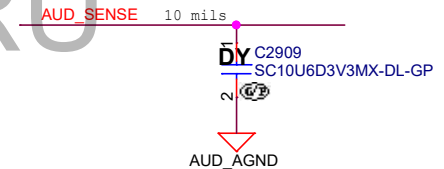
AUD\_SPK\_L- C 1  
AUD\_SPK\_L+ C 1  
AUD\_SPK\_R- C 1  
AUD\_SPK\_R+ C 1

AFTP2901  
AFTP2902  
AFTP2903  
AFTP2904

27 LINE1\_VREFO <<<  
27 MIC2\_VREFO\_R <<<  
27,66 AUD\_HP1\_JACK\_L <<<  
27,66 AUD\_HP1\_JACK\_R <<<  
27 LINE1\_L >>>  
27 LINE1\_R >>>  
27,66 AUD\_SLEEVE <<<  
27,66 AUD\_RING <<<  
27,66 AUD\_SENSE <<<



20180911  
Vendor modify



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Title:

**Audio IO**

Size:  
A4

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>WASP 13" WHL-U</b>		Rev <b>A00</b>
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**LAN RTL8106**

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A4

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**WASP 13" WHL-U**

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Title

***XFOM&RJ45***

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A4

Document Number

***WASP 13" WHL-U***

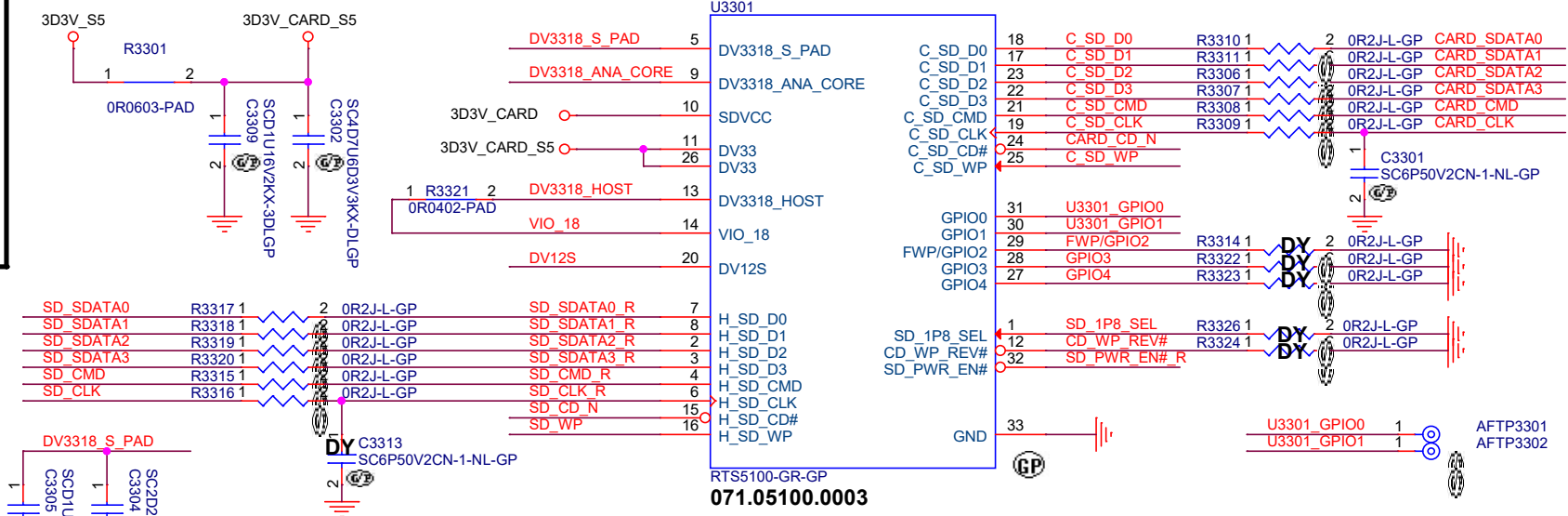
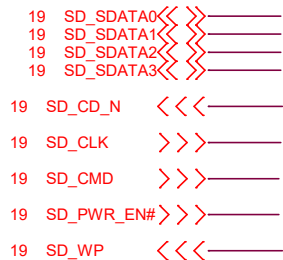
Rev

***A00***

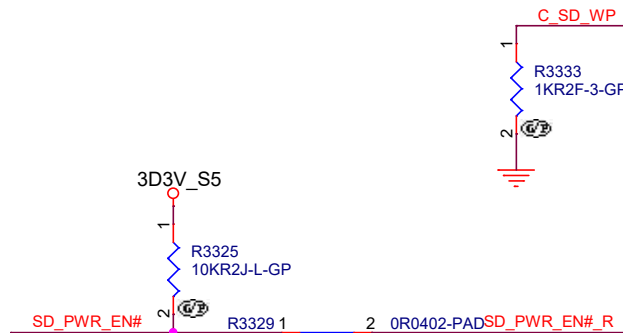
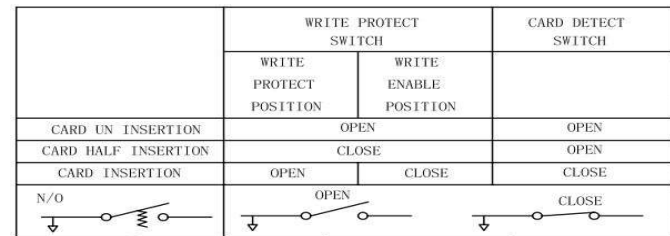
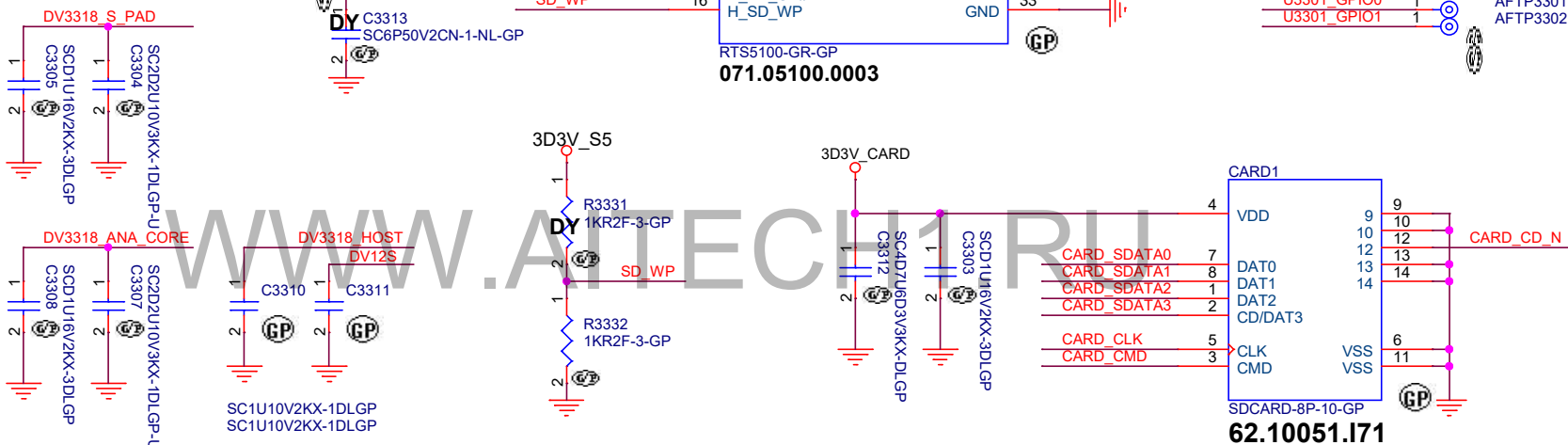
Date: Thursday, March 07, 2019

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## Main Func = Card Reader



NO.	PIN #	FUNCTION
1	#9	DAT2
2	#1	CD/DAT3
3	#2	CMD
4	#3-1	VSS
5	#3-2	VSS
6	#4	VDD
7	#5	CLD
8	CD	CARD DETECT
9	#6	VSS
10	#7	DAT0
11	#8	DAT1
12	WP1	WRITE PROTECT(VSS)
13	WP2	WRITE PROTECT(VDD)
14	FRAME	GND
15	FRAME	GND
16	FRAME	GND
17	FRAME	GND



## <Core Design>



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Title
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### Card Reader-RTS5100

Size

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## WASP 13" WHL-U

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SSID = USB3.0

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Title					
<b>USB switch</b>					
Size	Document Number				Rev
	<b>WASP 13" WHL-U</b>				<b>A00</b>
Date: Thursday, March 07, 2019		Sheet	35	of	106

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Title

**USB30**

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Title

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Rev

**A00**

Date: Thursday, March 07, 2019


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Main Func = USB3.0 Redriver

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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>USB30</b>					
Size	Document Number				Rev
A4	<b>WASP 13" WHL-U</b>				<b>A00</b>
Date: Thursday, March 07, 2019		Sheet 38		of 106	

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17	PM_SLP_S3#	>>>	_____
17,24,46	VCCST_PWRGD	<<<	_____
17,51,92	PM_SLP_S4#	>>>	_____
17,91	PM_SLP_S0#	>>>	_____
21	GPPC_H18_VCCIO_LPM	>>>	_____
24	ALWON	>>>	_____
24,53	PRIM_PWRGD	>>>	_____
26	PURE_HW_SHUTDOWN#	>>>	_____
45	3V_5V_EN	<<<	_____
51	PWR_VDDQ_PG	>>>	_____

**Power Good**

PWR\_VDDQ\_PG 1 2 VCCST\_PWRGD

R4011 OR402-PAD

3D3V\_S0 R4005 1K2J-1-GP

[#543016] Optional, Added for addition system robustness

NON DS3: PH 3V\_5V\_POK to 3D3V\_AUX\_S5 at page17

120V\_S3

C4007

SC1U02V2KX-3DLP

C4032

SC1U10V2KX-1DLG

5V\_S5

VCC25V\_EN RT

U4002

IN#1

IN#2

IN#3

VBIAS ON

GND

OUT#6

OUT#7

OUT#8

G5027RD1D-GP-U

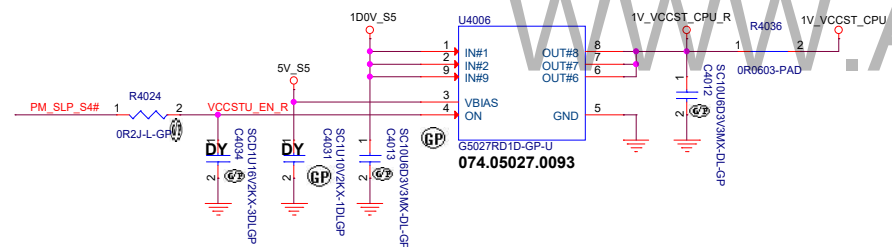
074.05027.0093

120V\_VCCSFR\_OC

C4007

SC1U16V2KX-3DLP

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

[illegible]

1D8V\_S5

C4037  
SCD1U16V2KX-3DLGP

R4034  
10KR2J-L-GP

C4038  
SC1U10V2KX-1DLGP

R4035  
20KR2J-1L-GP

Q4001  
2N7002K-2-GP

Q4002  
PJA3415-GP

1D8V\_S0 150mA

Q4039  
SCD1U16V2KX-3DLGP

PM\_SLP\_S3#

1D8V\_EN#

1D8V\_EN#

84.2N702.J31

084.03415.0031

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***Connected\_Standby(1/2)+DS3***

Size  
A4

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Title

***Connected\_Standby(2/2)***

Size  
A4

Document Number

**WASP 13" WHL-U**

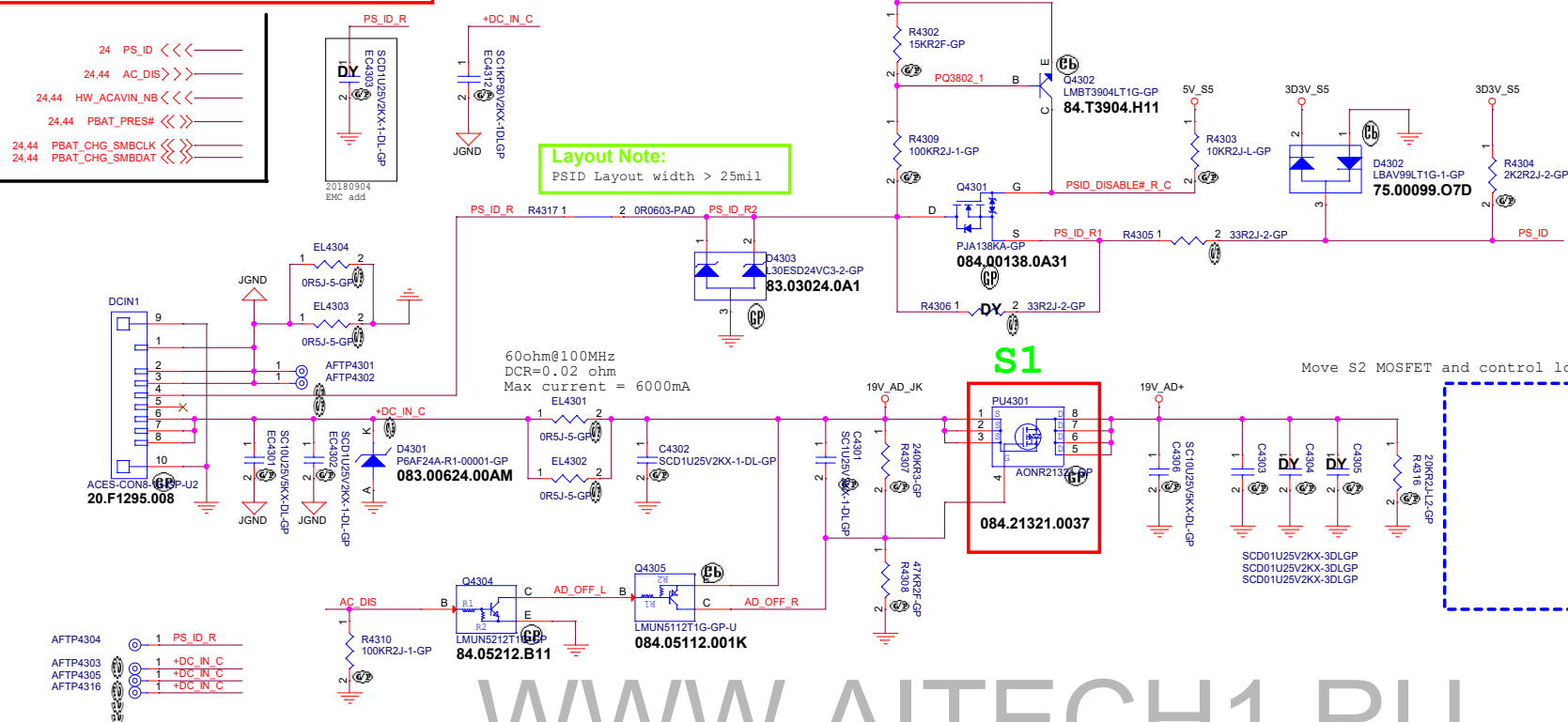
Rev

**A00**

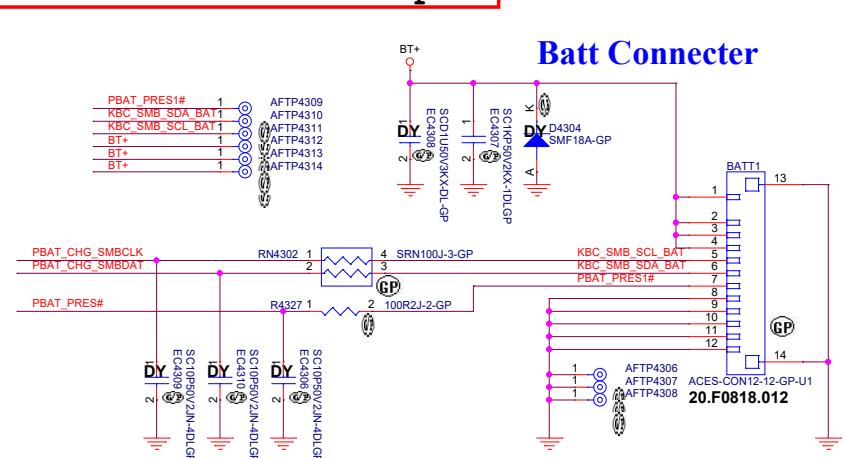
Date: Thursday, March 07, 2019

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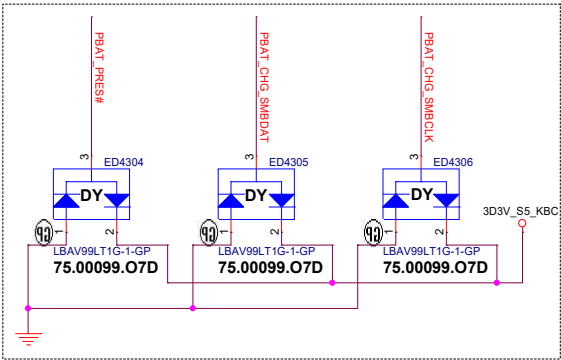
Main Func = ADT Input



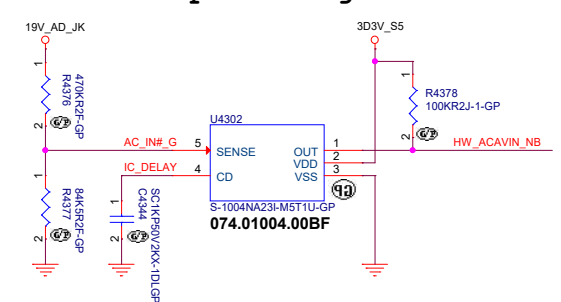
Main Func = M-BAT Input



Placement: Close to Batt Connector



Barrel Adapter Plug-in Detect



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File  
Spec A3 Document Number  
Date: Thursday, March 07, 2019

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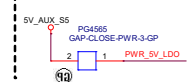
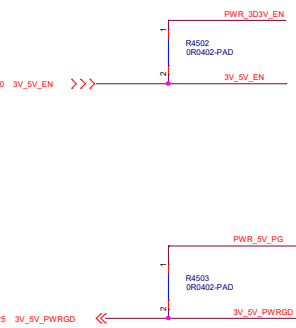
	ISL9538R	ISL9532Z
PR4468	100K(63.10434.1DL)	100K(64.R0005.6DL)
PC4469	1500p(78.13224.2FLDL)	DY
PQ4451	0R4.02421.0031	DY
PR4469	DY	0R(64.R0005.6DL)
PR4441	DY	0R(64.R0005.6DL)
PR4440	0R(64.R0005.6DL)	DY
PR4471	0R(64.R0005.6DL)	DY
PR4470	DY	0R(64.R0005.6DL)



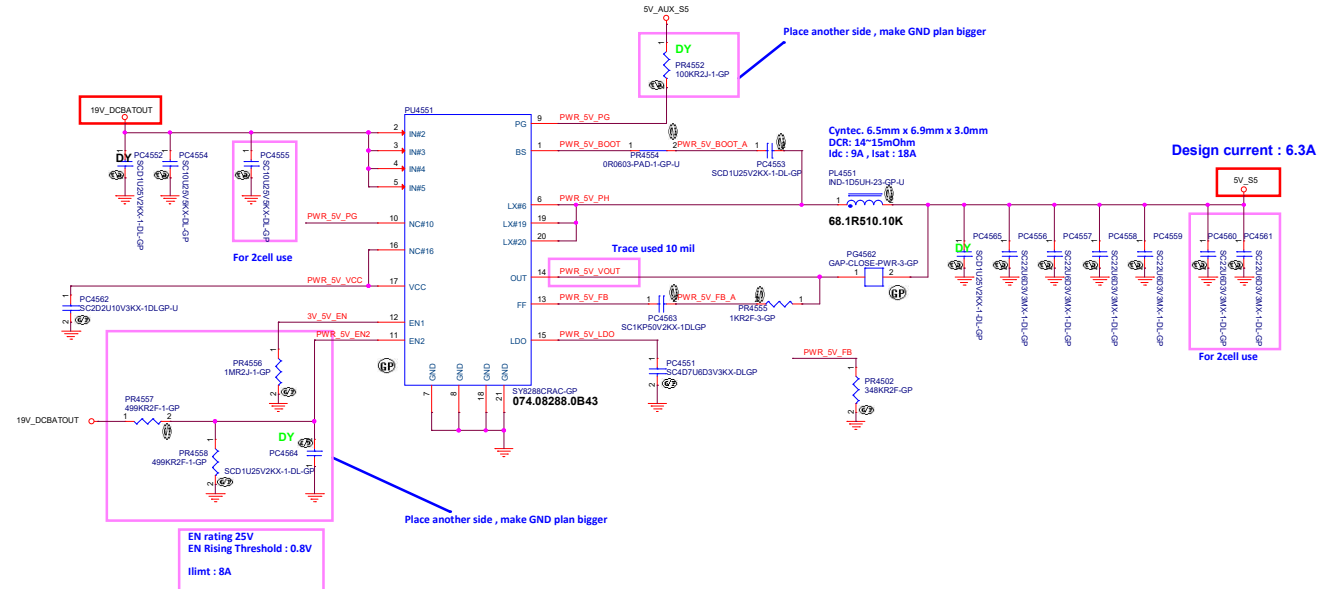
SSID = PWR.Plane.Regulator\_5V

OFFPAGE-Signal

OFFPAGE-GAP



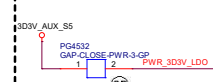
# SY8288C For 5V



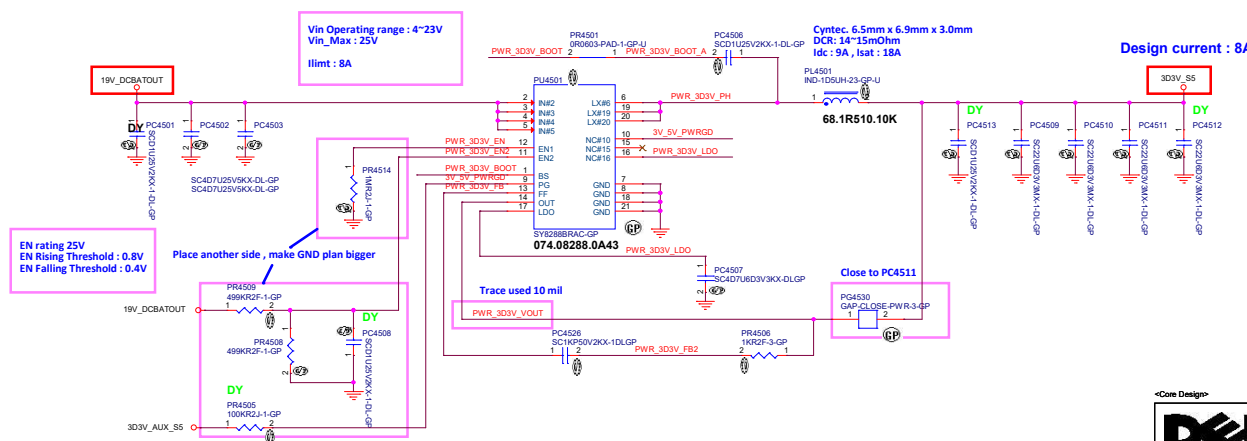
SSID = PWR.Plane.Regulator\_3D3V

OFFPAGE-Signal

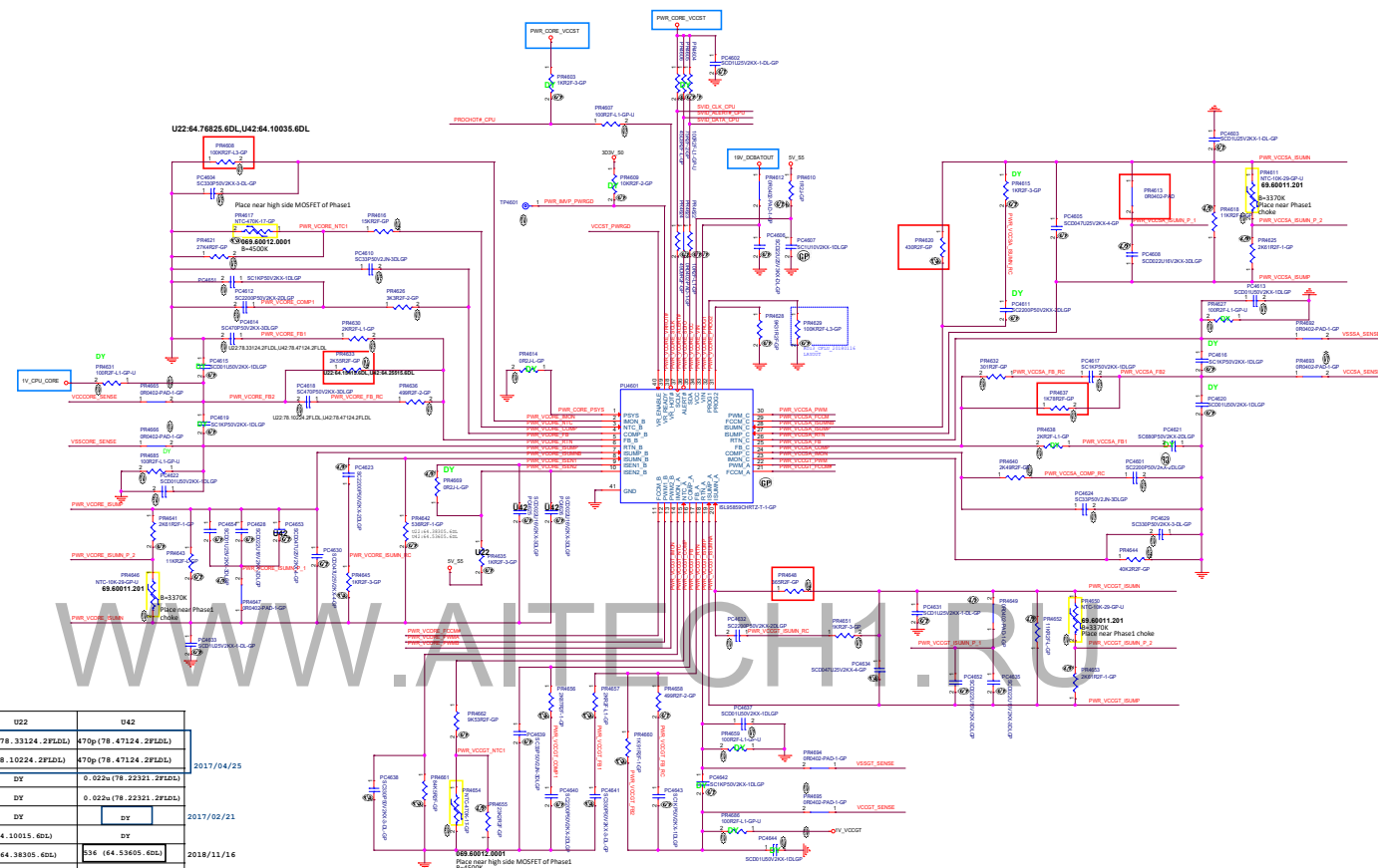
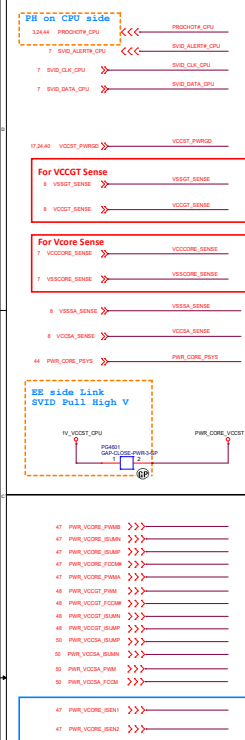
OFFPAGE-GAP



# SY8288B For 3D3V



# ISL95859C For CPUCORE



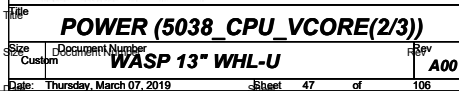
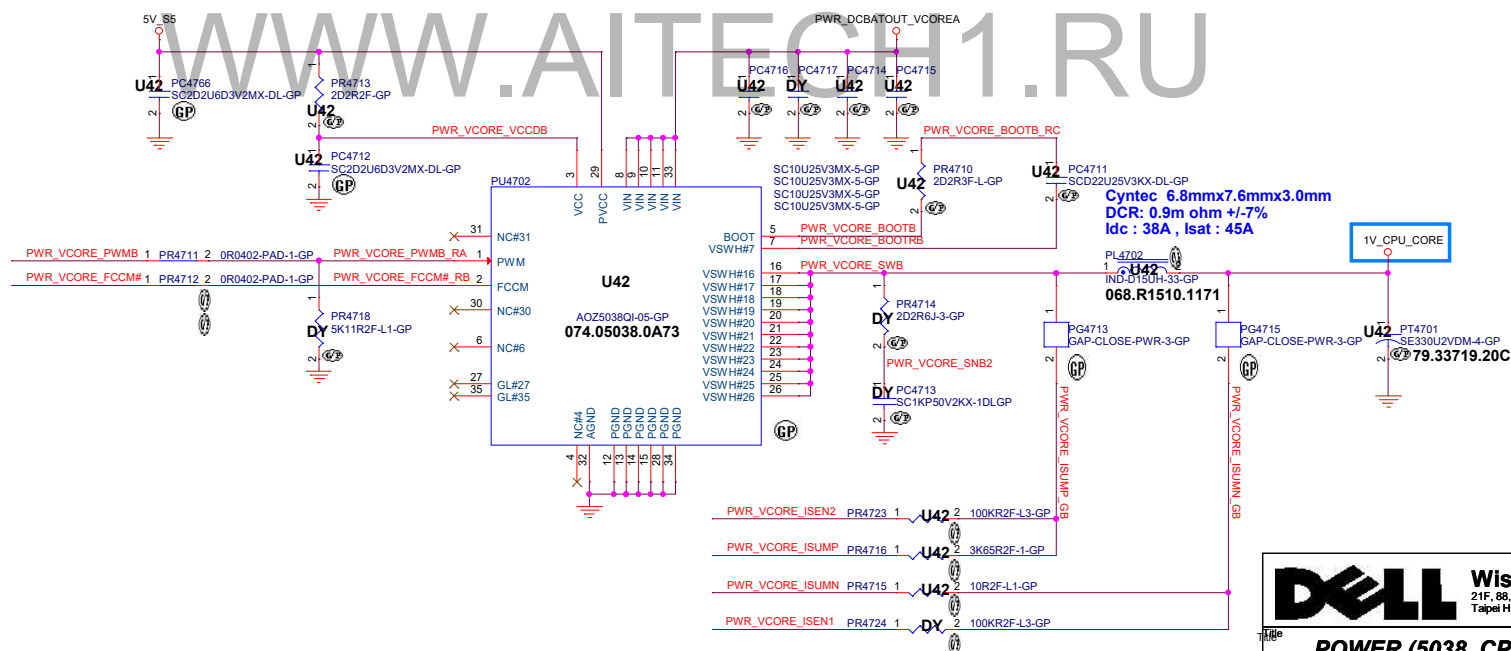
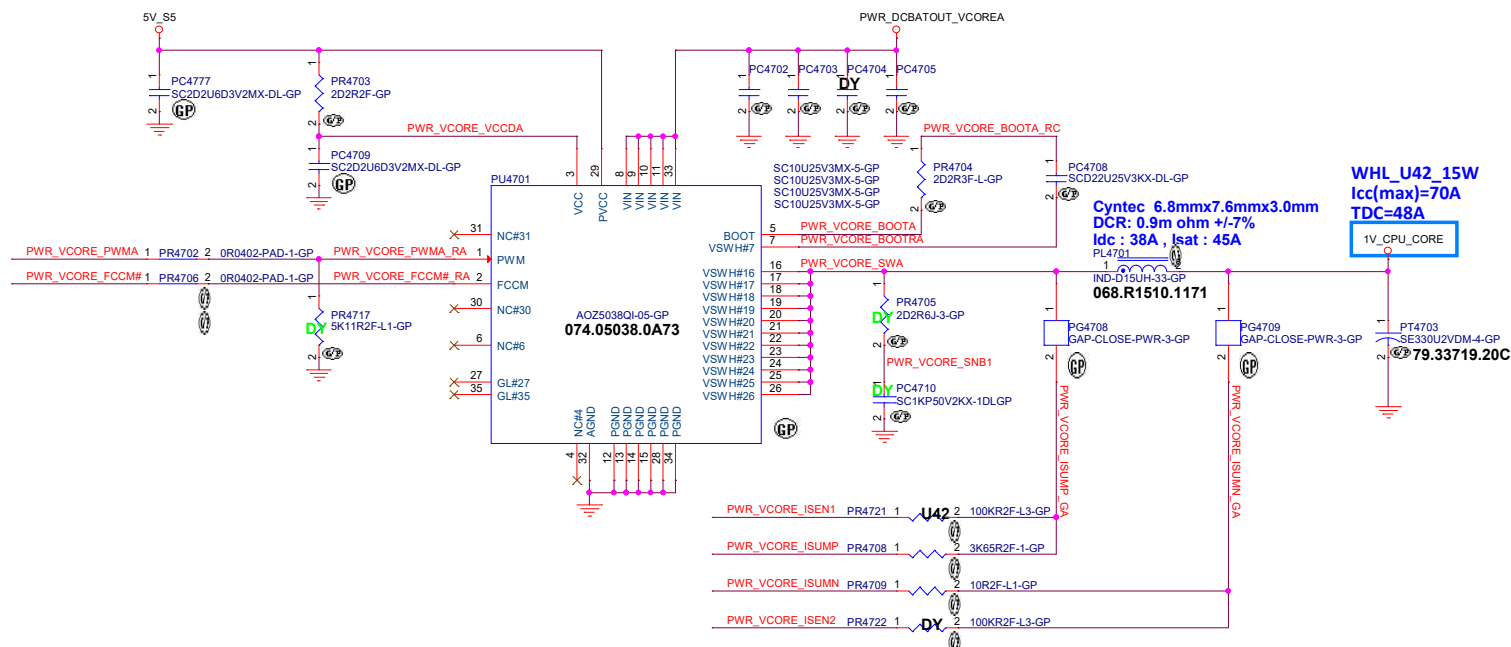
	U22	U42	
PC4614	330P (78. 2124. 2FLDL)	470p (78. 47124. 2FLDL)	2017/04/25
PC4618	38P (78. 10224. 2FLDL)	470p (78. 47124. 2FLDL)	
PC4625		0. 022h (78. 22321. 2FLDL)	
PC4626	DY	0. 022h (78. 22321. 2FLDL)	2017/02/21
PR4669	DY	DY	
PR4635	1X (64. 10015. 6DL)	DY	
PC4642	383 (64. 38305. 6DL)	536 (64. 53605. 6DL)	2018/11/16
PC4640	472w (78. 47322. 02PD)	472w (78. 47322. 02PD)	
PC4628	22w (78. 22321. 2FLDL)	22w (78. 22321. 2FLDL)	
PC4654	10w (78. 10322. 2FLDL)	10w (78. 10322. 2FLDL)	2018/11/16
PC4653	DY	472w (78. 47322. 02PD)	
PC4633	1. 54K (64. 15415. 0DL)	2. 55K (64. 25515. 0DL)	
PR4608	76. 8K (64. 76815. 0DL)	64. 0 (64. 10035. 6DL)	

PWR\_DCBATOUT\_VCOREA

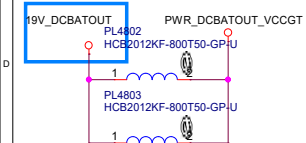
TC4702

SE33U25VM-11-GP

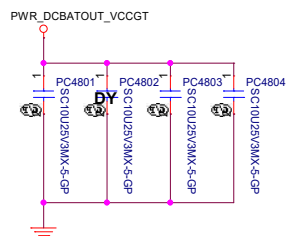
79.33612.20L



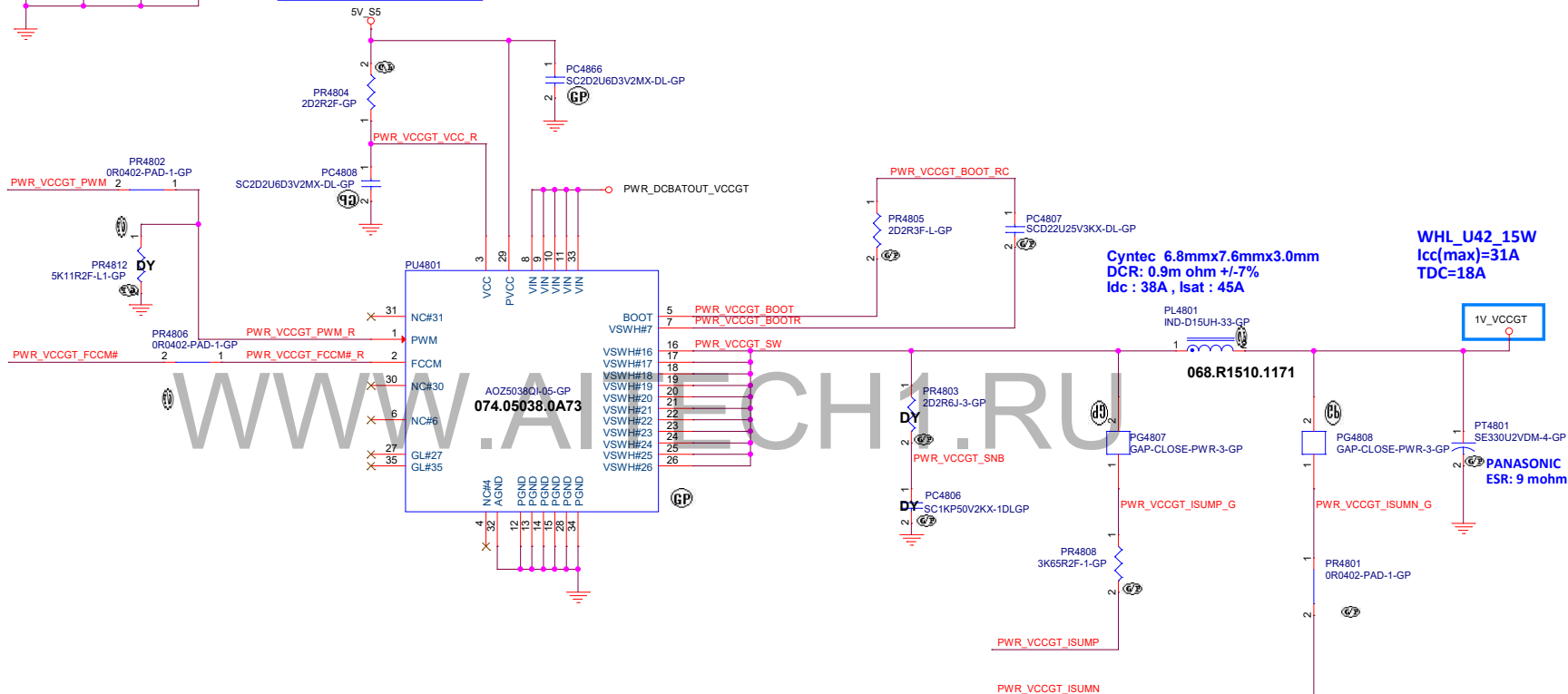
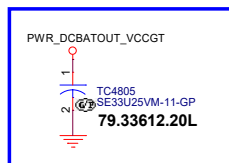
Offpage-Signal



46 PWR\_VCCGT\_PWM  
46 PWR\_VCCGT\_FCCM#  
46 PWR\_VCCGT\_ISUMP  
46 PWR\_VCCGT\_ISUMN



For acoustic noise



***RSVD***

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Title

***POWER (CPU VCCGTS RSVD)***

Size

A3

Document Number

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Rev

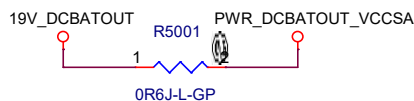
***A00***

Date: Thursday, March 07, 2019

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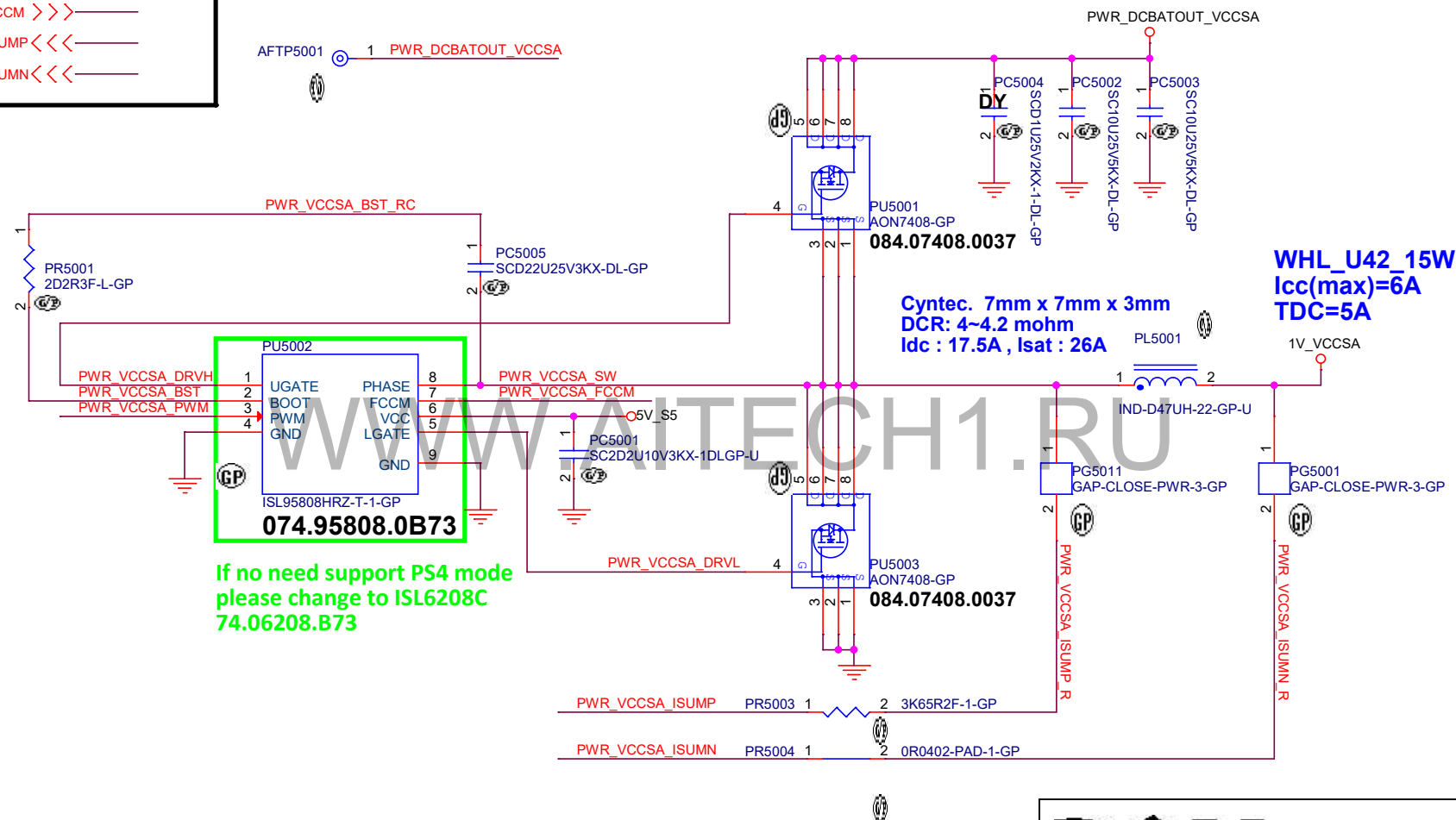
Main Func = CPU CORE

## OFFPAGE



46 PWR\_VCCSA\_PWM >>> \_\_\_\_\_  
46 PWR\_VCCSA\_FCCM >>> \_\_\_\_\_  
46 PWR\_VCCSA\_ISUMP <<< \_\_\_\_\_  
46 PWR\_VCCSA\_ISUMN <<< \_\_\_\_\_

# ISL95808 For VCCSA



If no need support PS4 mode  
please change to ISL6208C  
74.06208.B73



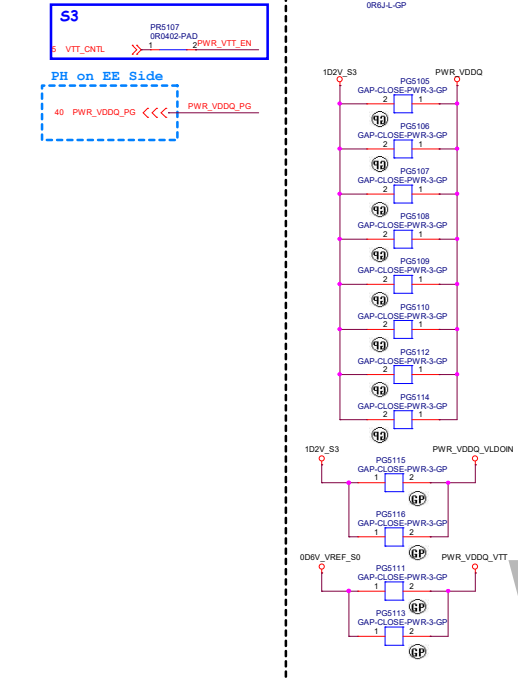
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Title <b>POWER (ISL95808_VCCSA)</b>		
Size A4	Document Number <b>WASP 13" WHL-U</b>	Rev <b>A00</b>
Date: Thursday, March 07, 2019 Sheet 50 of 106		

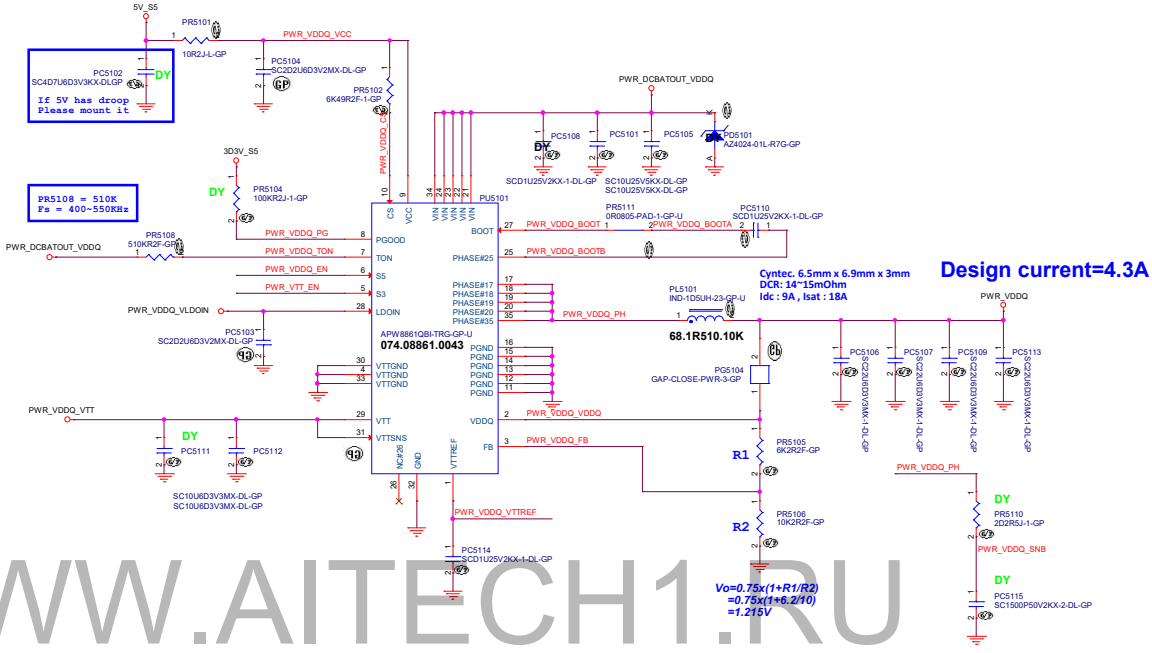
SSID = PWR.Plane.Regulator\_1D2V/0D6V

OFFPAGE-Signal

OFFPAGE-GAP



# G5388 For VDDQ/VTT



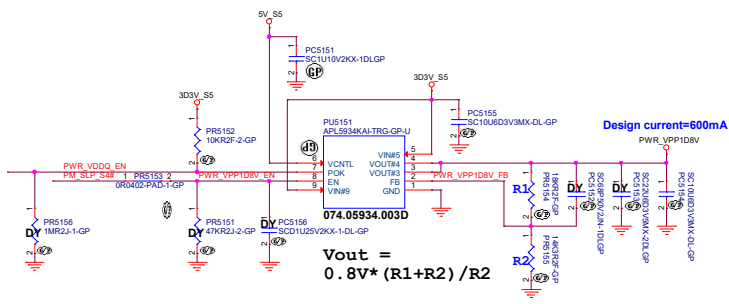
SSID = PWR.Plane.Regulator\_1D8V

OFFPAGE-Signal

OFFPAGE-GAP



# APL5934 For 1D8V

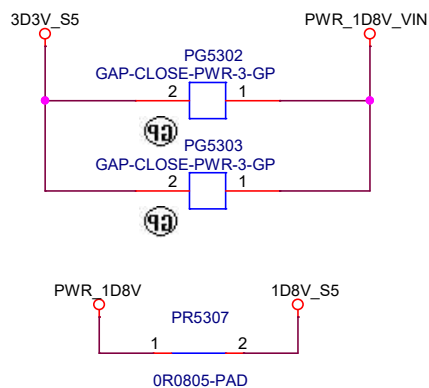




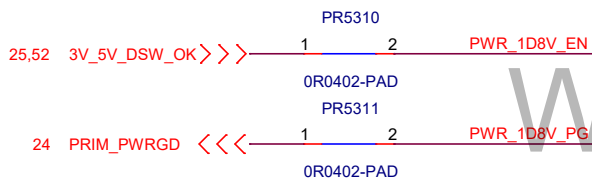


Main Func = 1D8V

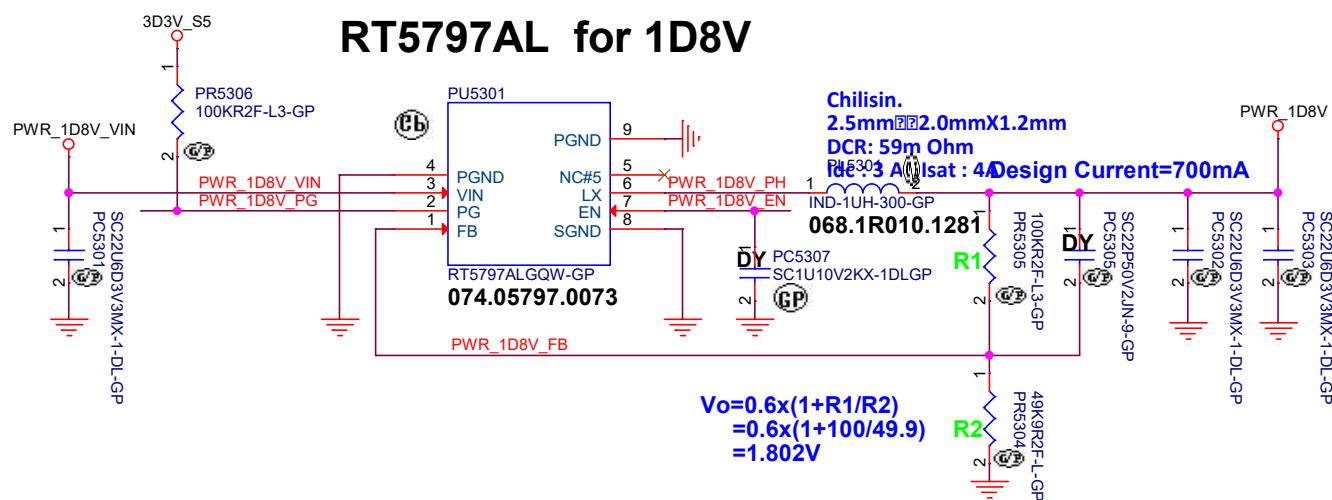
## OFFPAGE\_GAP



## OFFPAGE



## RT5797AL for 1D8V



$$V_o = 0.6 \times (1 + R1/R2) \\ = 0.6 \times (1 + 100/49.9) \\ = 1.802V$$

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Title:

**POWER (APL5934\_1D8V)**

Size:  
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Document Number

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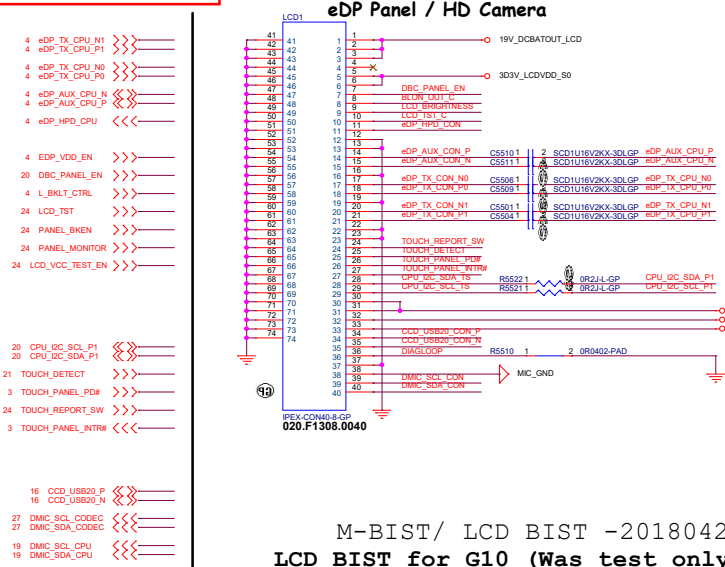
Rev

**A00**

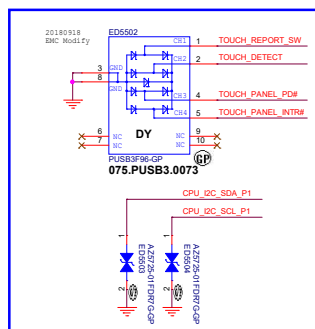
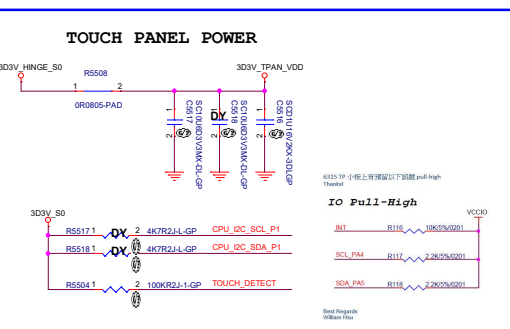
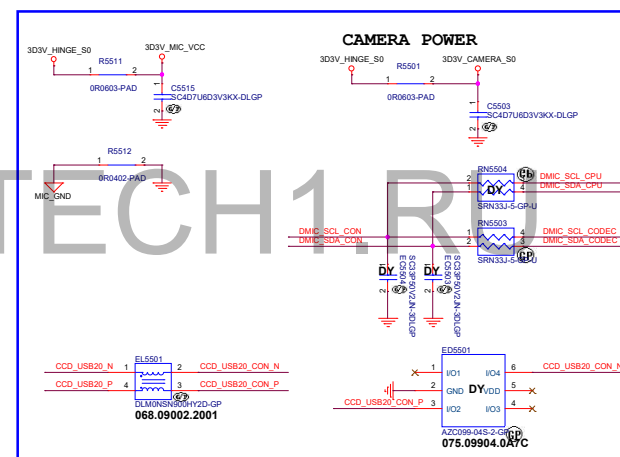
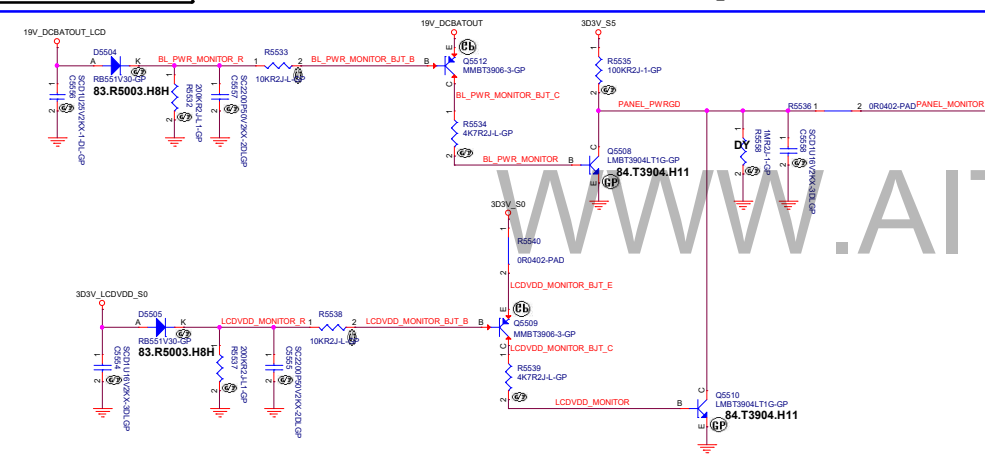
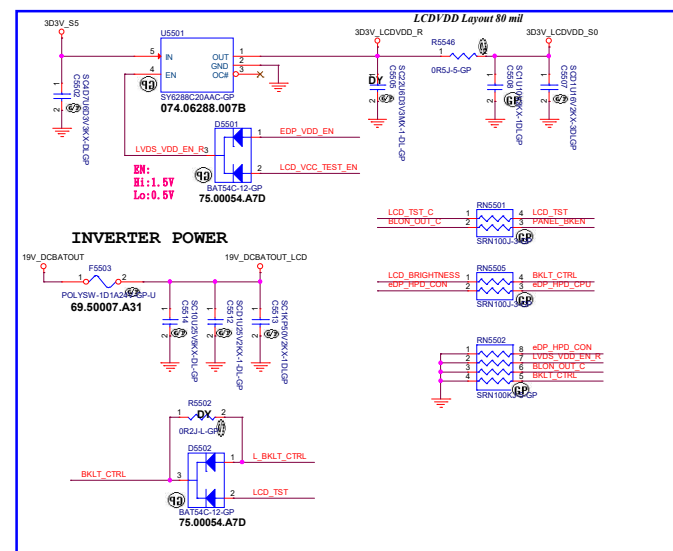
Date: Thursday, March 07, 2019

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**Main Func = LCD**




M-BIST/ LCD BIST -20180425  
LCD BIST for G10 (Was test only for G9)



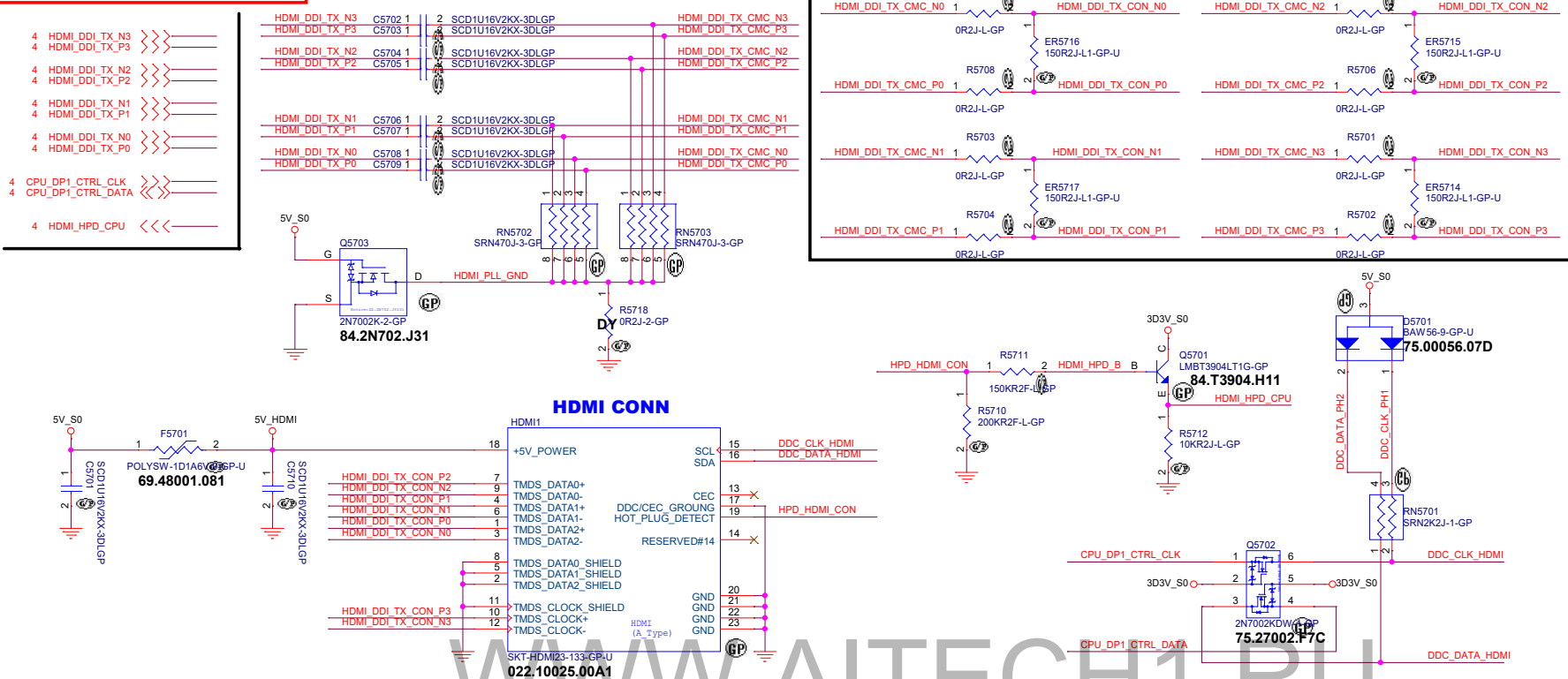
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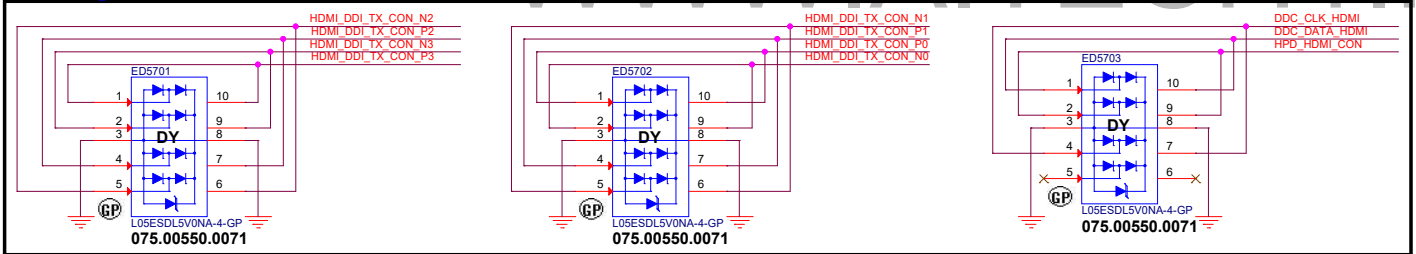
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>CRT</b>		
Size A4	Document Number <b>WASP 13" WHL-U</b>	Rev <b>A00</b>
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Main Func = HDMI



EMI Request:



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Size  
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**WASP 13" WHL-U**

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Title

**SATA IF HDD/ODD**

Size  
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Document Number

**WASP 13" WHL-U**

Rev

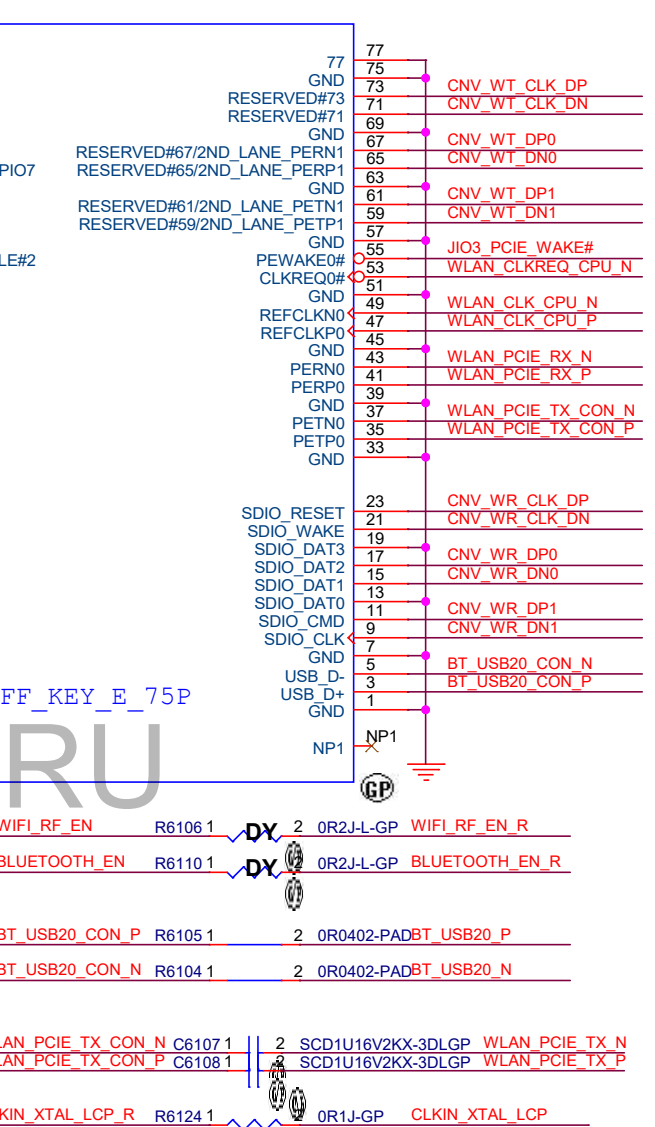
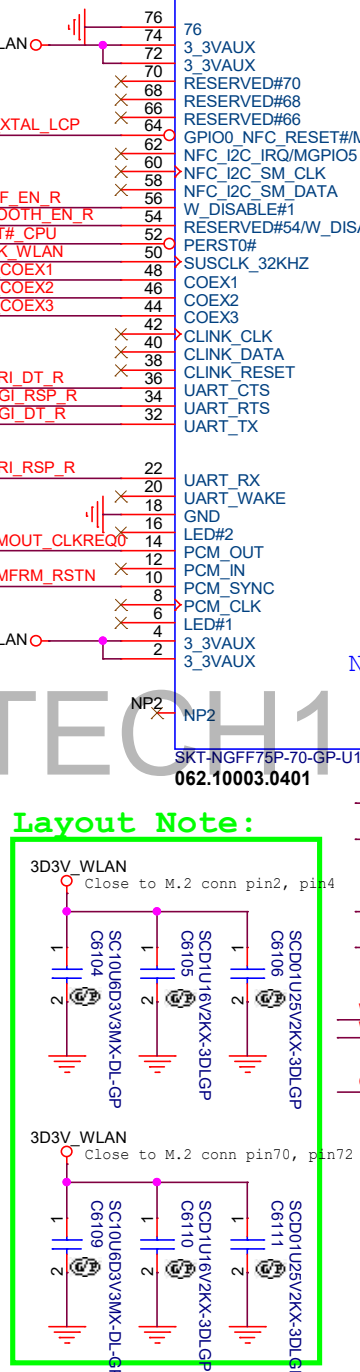
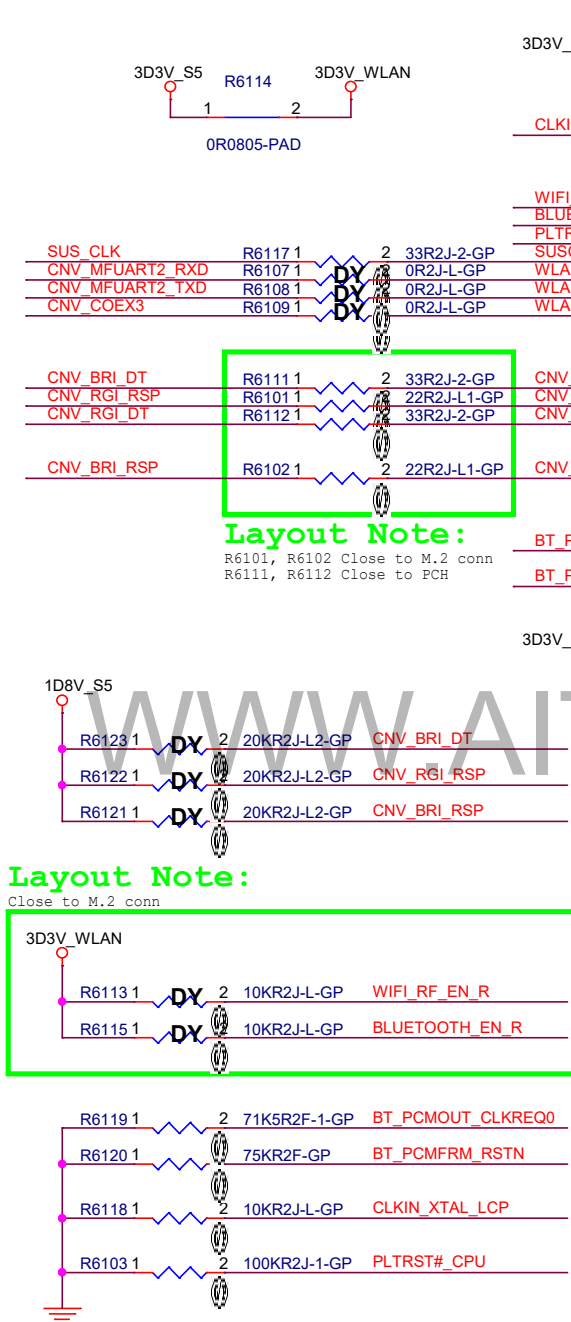
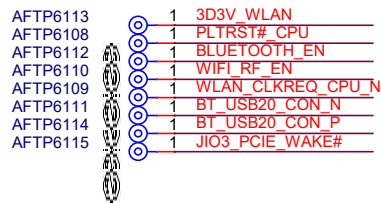
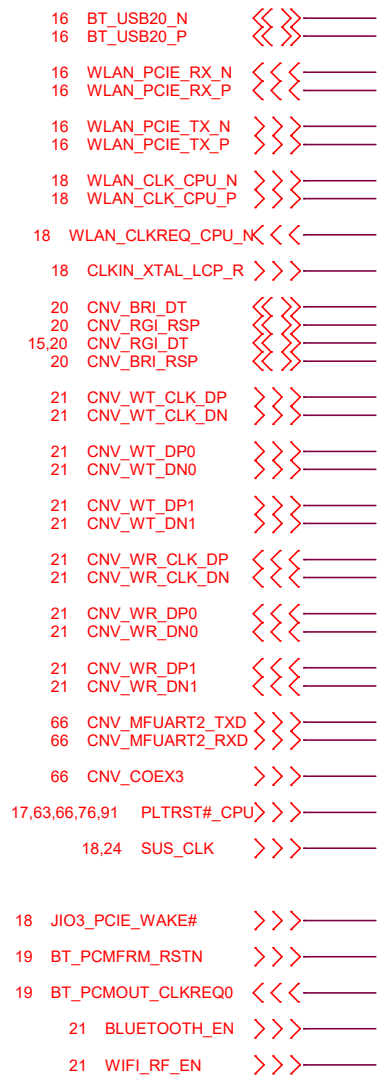
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## Main Func = WLAN



 <div> <b>Wistron Corporation</b>            21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,            Taipei Hsien 221, Taiwan, R.O.C.         </div>	
<b>Title</b> <div> <b>NGFF WLAN CONN</b>  <b>WASP 13" WHL-U</b> </div>	
<b>Size</b> A4	<b>Document Number</b> <b>A00</b>
<b>Date:</b> Thursday, March 07, 2019	
<b>Sheet</b> 61 of 106	

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Title

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Size  
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**A00**

Date: Thursday, March 07, 2019

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Main Func = SSD M.2

16	SSD_PCIE_TX_N3	>>>
16	SSD_PCIE_TX_P3	<<<
16	SSD_PCIE_RX_N3	<<<
16	SSD_PCIE_RX_P3	>>>
16	SSD_PCIE_TX_N2	>>>
16	SSD_PCIE_TX_P2	<<<
16	SSD_PCIE_RX_N2	<<<
16	SSD_PCIE_RX_P2	>>>
16	SSD_PCIE_TX_N1	>>>
16	SSD_PCIE_TX_P1	<<<
16	SSD_PCIE_RX_N1	<<<
16	SSD_PCIE_RX_P1	>>>
16	SSD_SATA_TX_N	>>>
16	SSD_SATA_TX_P	<<<
16	SSD_SATA_RX_N	<<<
16	SSD_SATA_RX_P	>>>
18	SSD_CLK_CPU_P	>>>
18	SSD_CLK_CPU_N	<<<
18	SSD_CLKREQ_CPU_N	<<<
16	SSD_DEVS_L_P	>>>
24,66	SSD_SCP#	>>>
17,61,66,76,91	PLTRSTR_CPU	>>>
64,66	M2_PCIE_LED#	<<<
16	M2_SSD_PEDET	<<<

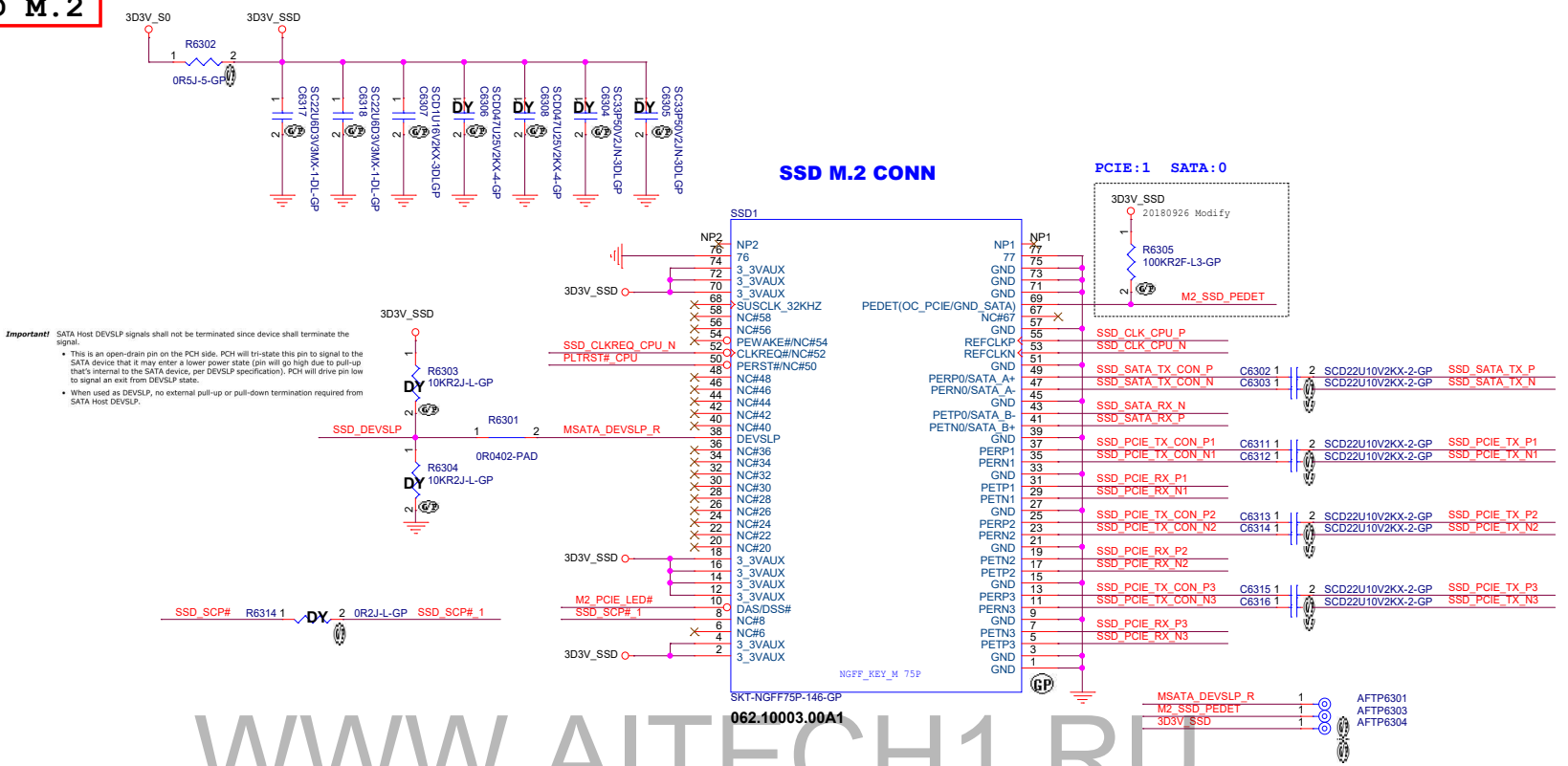


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

34	NC	NC	75
72	NC	NC	73
74	NC	NC	71
76	NC	NC	69
78	NC	NC	67
80	NC	NC	65
82	NC	NC	63
84	NC	NC	61
86	NC	NC	59
88	NC	NC	57
90	NC	NC	55
92	NC	NC	53
94	NC	NC	51
96	NC	NC	49
98	NC	NC	47
100	NC	NC	45
102	NC	NC	43
104	NC	NC	41
106	NC	NC	39
108	NC	NC	37
110	NC	NC	35
112	NC	NC	33
114	NC	NC	31
116	NC	NC	29
118	NC	NC	27
120	NC	NC	25
122	NC	NC	23
124	NC	NC	21
126	NC	NC	19
128	NC	NC	17
130	NC	NC	15
132	NC	NC	13
134	NC	NC	11
136	NC	NC	9
138	NC	NC	7
140	NC	NC	5
142	NC	NC	3
144	NC	NC	1

Table 13-11.SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe\* lane that needs to support either **PCIe\* Gen2 devices** or **PCIe\* Gen3 devices**, follow the PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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File: **SSD M.2eMMC**

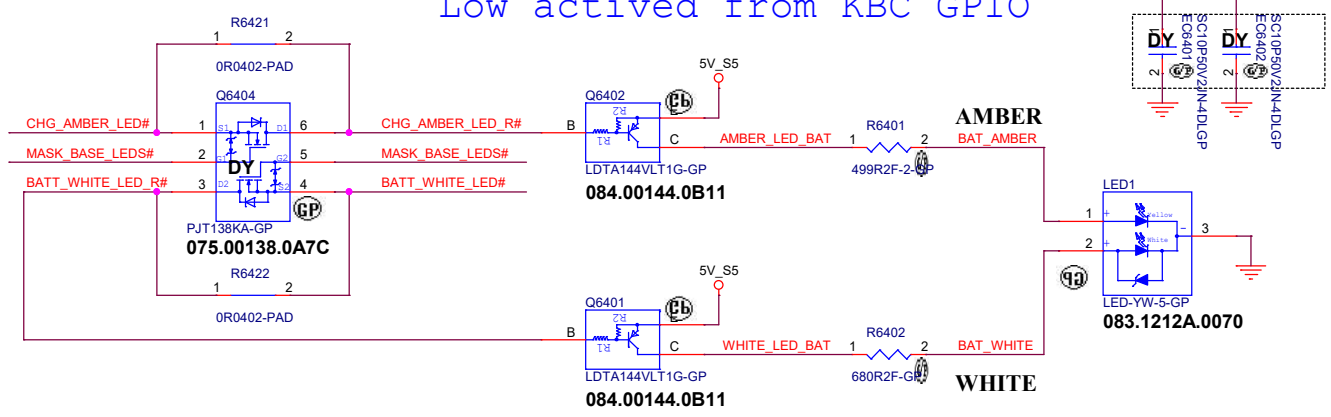
Spec: A3 Document Number: **WASP 13" WHL-U** Rev: **A00**

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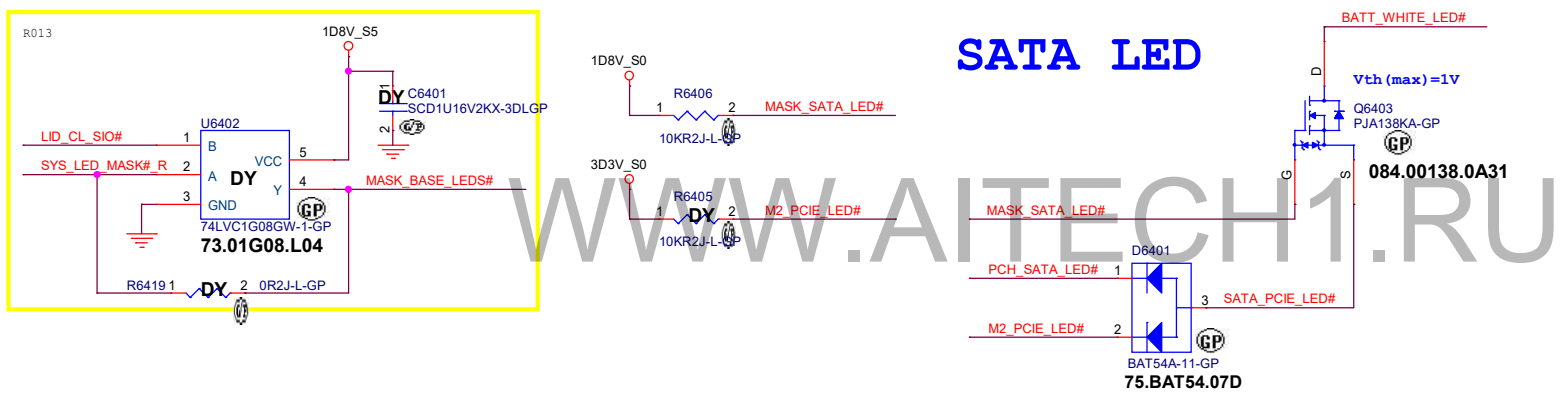
**Main Func = Power BTN**

- 24 CHG\_AMBER\_LED# >>>
- 24 BATT\_WHITE\_LED# >>>
- 24 SYS\_LED\_MASK#\_R >>>
- 16 PCH\_SATA\_LED# >>>
- 63,66 M2\_PCIE\_LED# >>>
- 20,24,67,92 LID\_CL\_SIO# >>>
- 24 MASK\_SATA\_LED# >>>
- 24,92 KBC\_PWRBTN# >>>
- 24,44 HW\_ACAV\_IN >>>
- 17,24 PCH\_RSMRST# >>>
- 24 EC\_D\_INHIB >>>

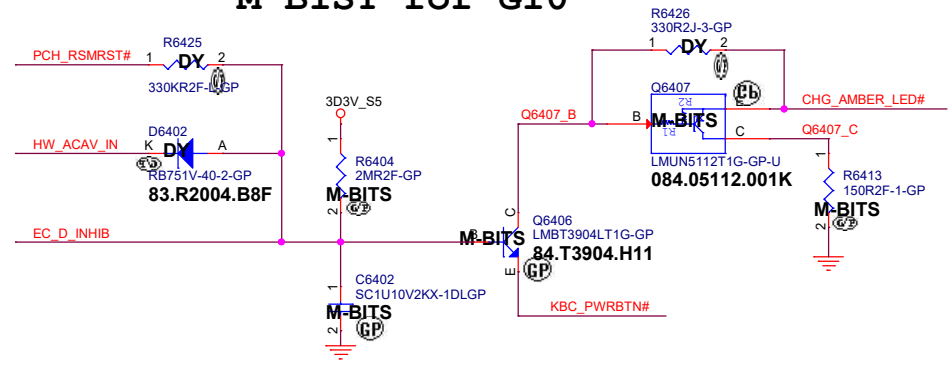
**Battery LED1 (AMBER\_LED)**  
Low actived from KBC GPIO



**Battery LED2 (WHITE\_LED)**  
Low actived from KBC GPIO



**M-BIST for G10**



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

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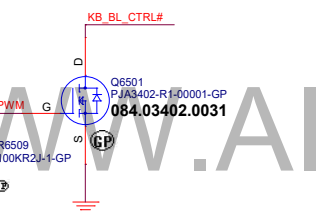
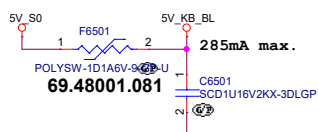
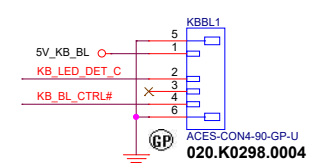
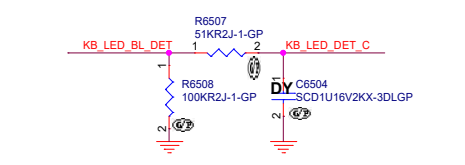
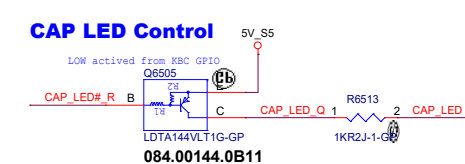
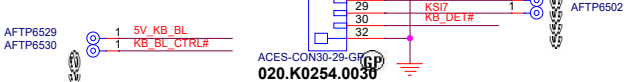
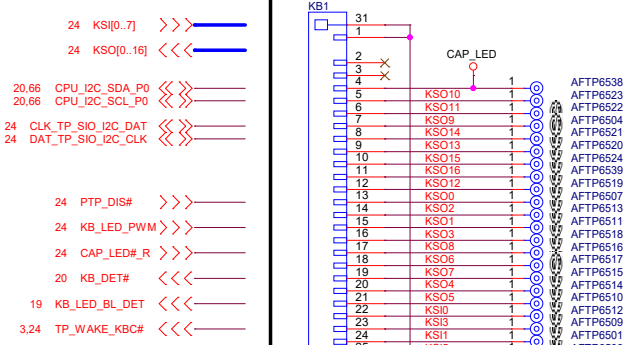
Title **LED Board&Power Button**

Size Custom Document Number **WASP 13" WHL-U** Rev **A00**

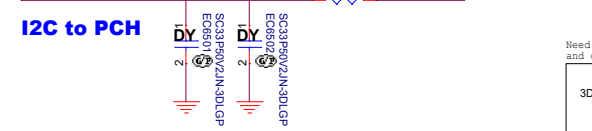
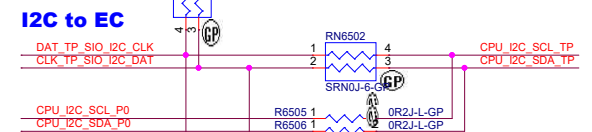
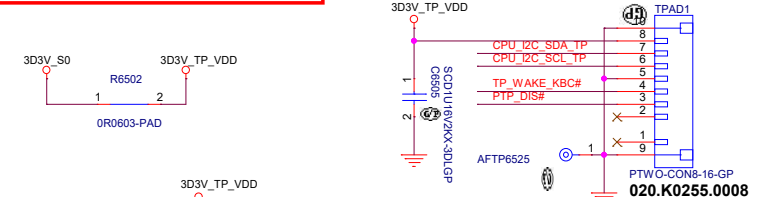
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SSID = KB

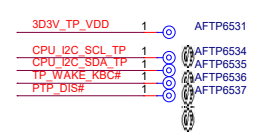
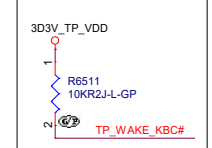
Main Func = Keyboard



Main Func = TPAD

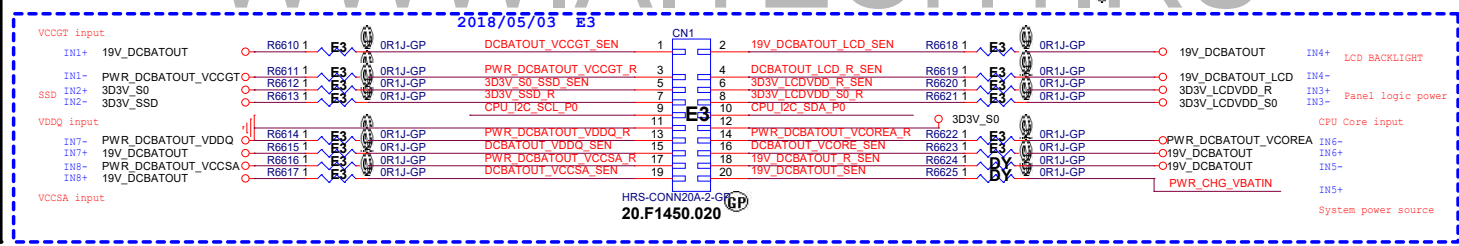
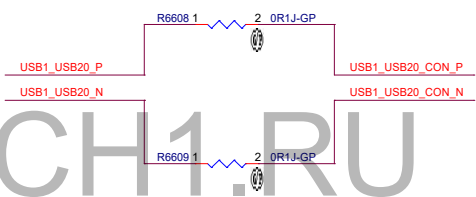
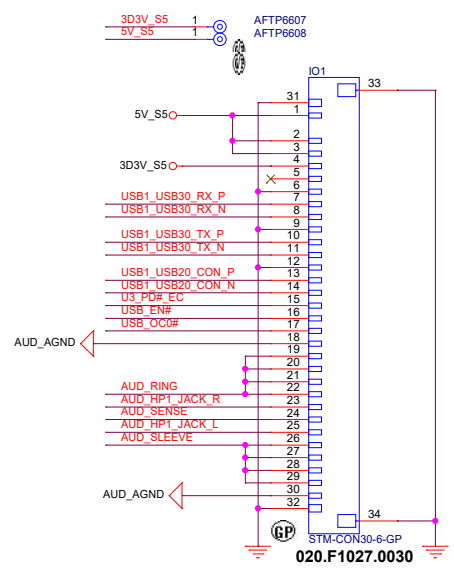
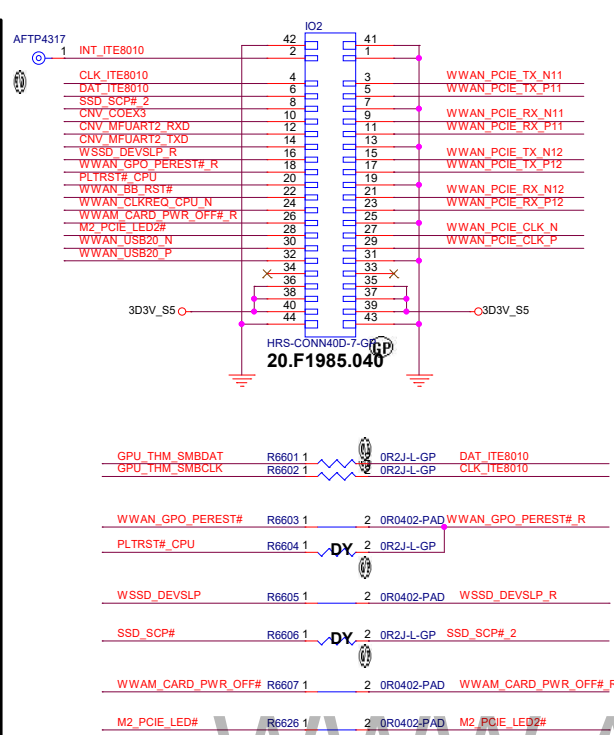
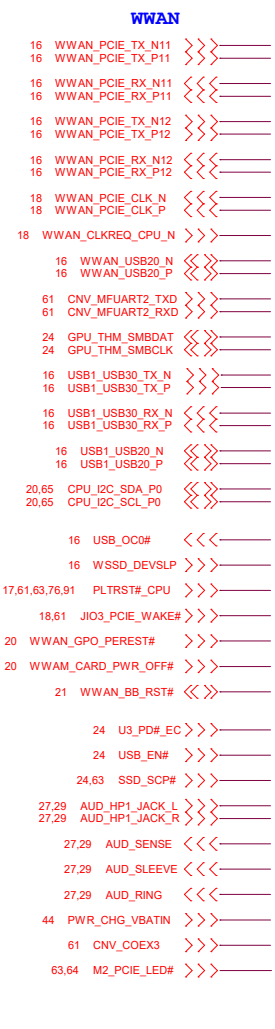


Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



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Main Func = IO Connector



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Title **IO Board Connector**

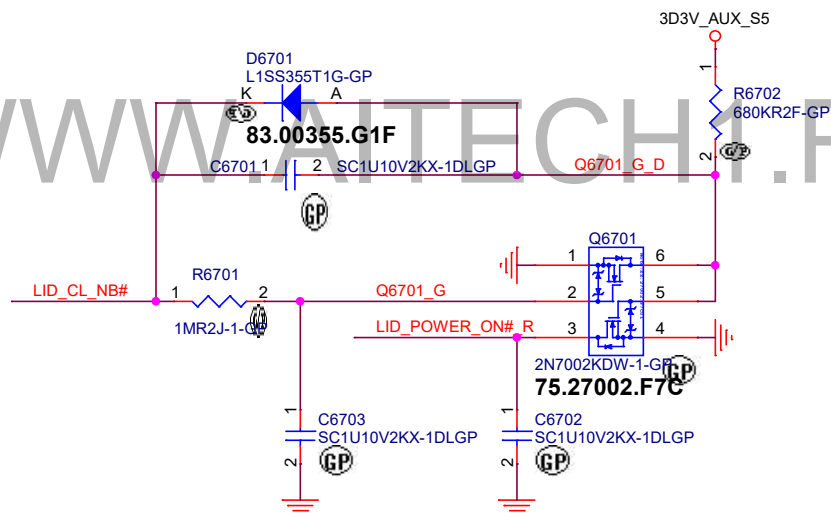
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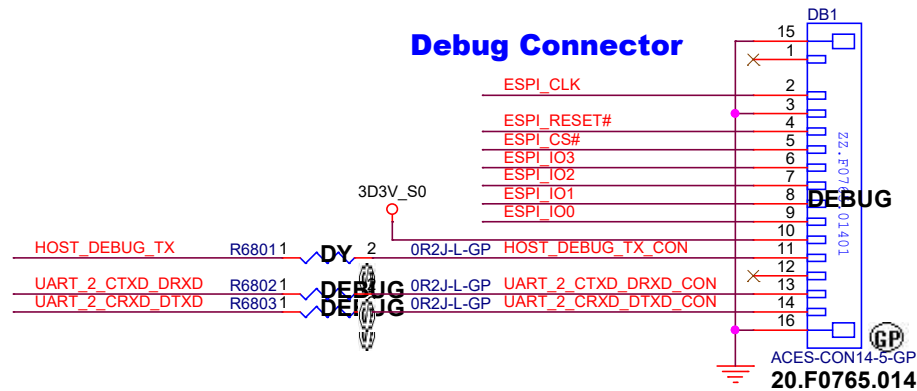
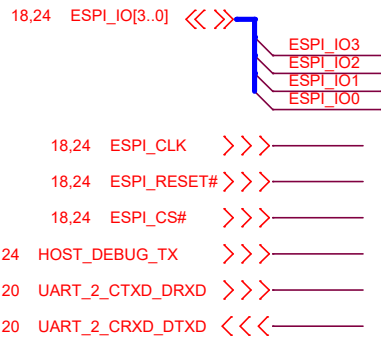
24  LID_POWER_ON#_R  >>>_____
20,24,64,92  LID_CL_SIO#  <<<_____

```

[illegible]

Title			
<b>Sensor (Hall-Sensor)</b>			
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# Main Func = Debug



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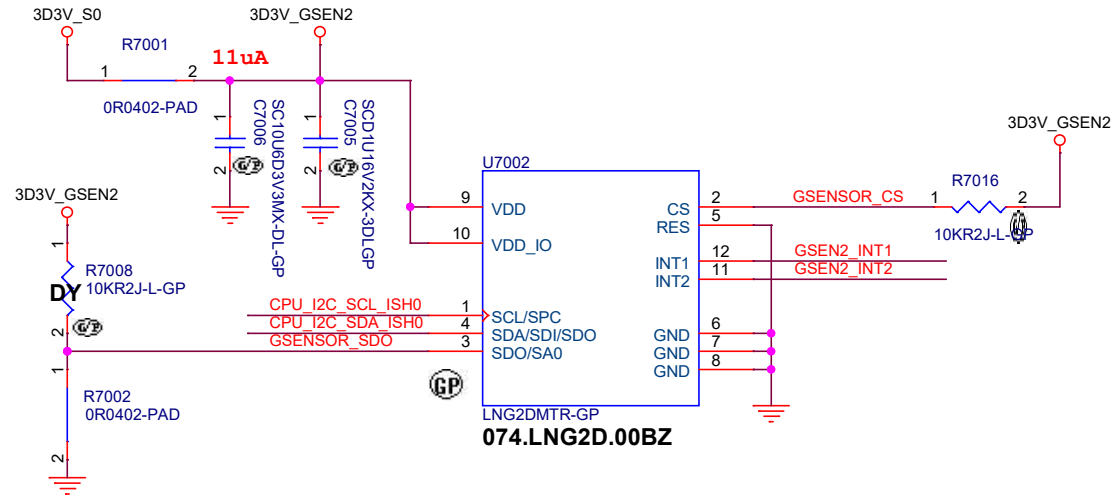
**A00**

Date: Thursday, March 07, 2019

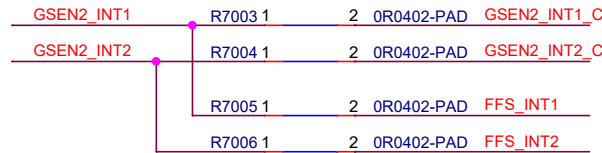
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# Main Func = G-sensor

20 GSEN2\_INT1\_C <<<<  
20 GSEN2\_INT2\_C <<<<  
  
18 FFS\_INT1 <<<<  
20 FFS\_INT2 <<<<  
  
20 CPU\_I2C\_SCL\_ISH0 <<<<  
20 CPU\_I2C\_SDA\_ISH0 <<<<



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Title

**Sensor**

Size  
A4

Document Number

**WASP 13" WHL-U**

Rev  
A00

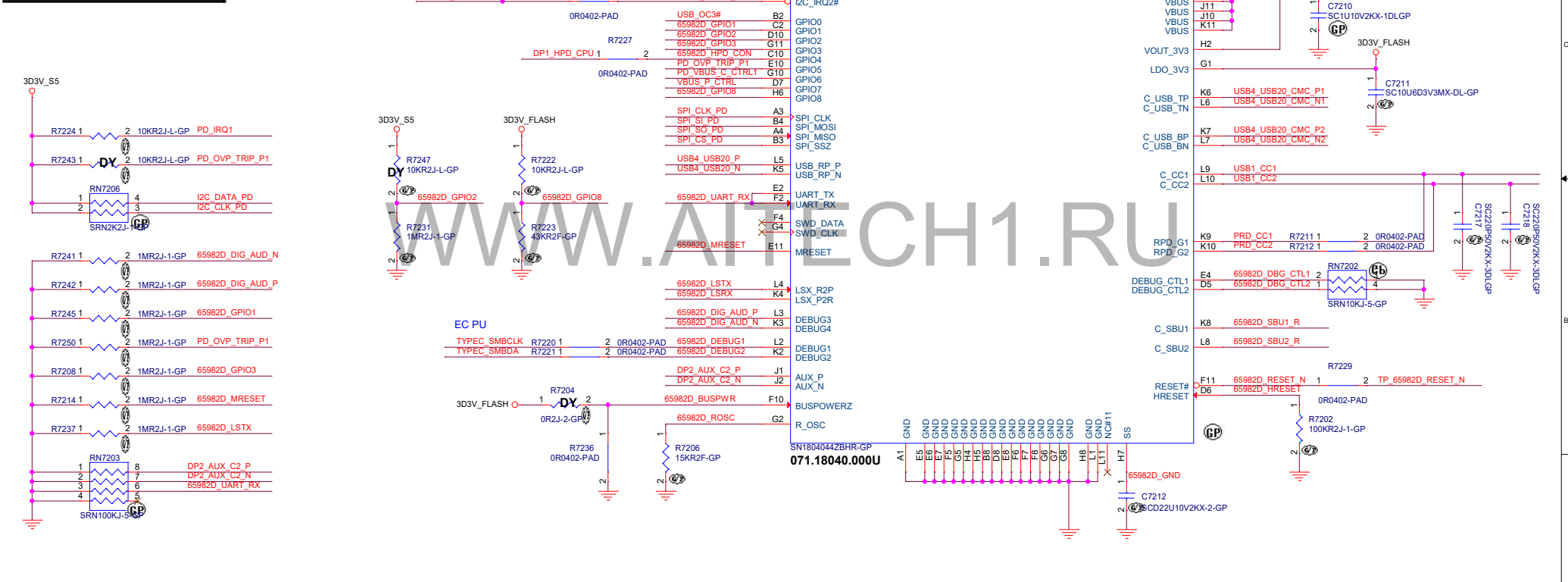
Date: Thursday, March 07, 2019

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Date: Thursday, March 07, 2019 Sheet 71 of 106

Main Func = TPS65982DC

- 4,71 DP1\_HPD\_CPU <<<
- 74 PD\_VBUS\_C\_CTRL1 <<<
- 74 VBUS\_P\_CTRL <<<
- 16 USB\_OC3# <<<
- 24 UPD1\_SMBINT# <<<
- 71 I2C\_CLK\_PD <<<
- 71 I2C\_DATA\_PD <<<
- 24 TYPEC\_SMBDA <<<
- 24 TYPEC\_SMBCLK <<<
- 73 USB1\_CC1 <<<
- 73 USB1\_CC2 <<<
- 73 USB4\_USB20\_CON\_N1 <<<
- 73 USB4\_USB20\_CON\_P1 <<<
- 73 USB4\_USB20\_CON\_N2 <<<
- 73 USB4\_USB20\_CON\_P2 <<<
- 16 USB4\_USB20\_P <<<
- 16 USB4\_USB20\_N <<<



USB4\_USB20\_CMC\_N1 1 EL7201 2 USB4\_USB20\_CON\_N1

USB4\_USB20\_CMC\_P1 4 EL7201 3 USB4\_USB20\_CON\_P1

DLMONSNG0HY2D-GP 068.09002.2001

USB4\_USB20\_CMC\_N2 1 EL7202 2 USB4\_USB20\_CON\_N2

USB4\_USB20\_CMC\_P2 4 EL7202 3 USB4\_USB20\_CON\_P2

DLMONSNG0HY2D-GP 068.09002.2001

65982D\_LSRX 1 TP7202

65982D\_SBU1\_R 1 TP7203

65982D\_SBU2\_R 1 TP7204

TP\_65982D\_RESET\_N 1 TP7205

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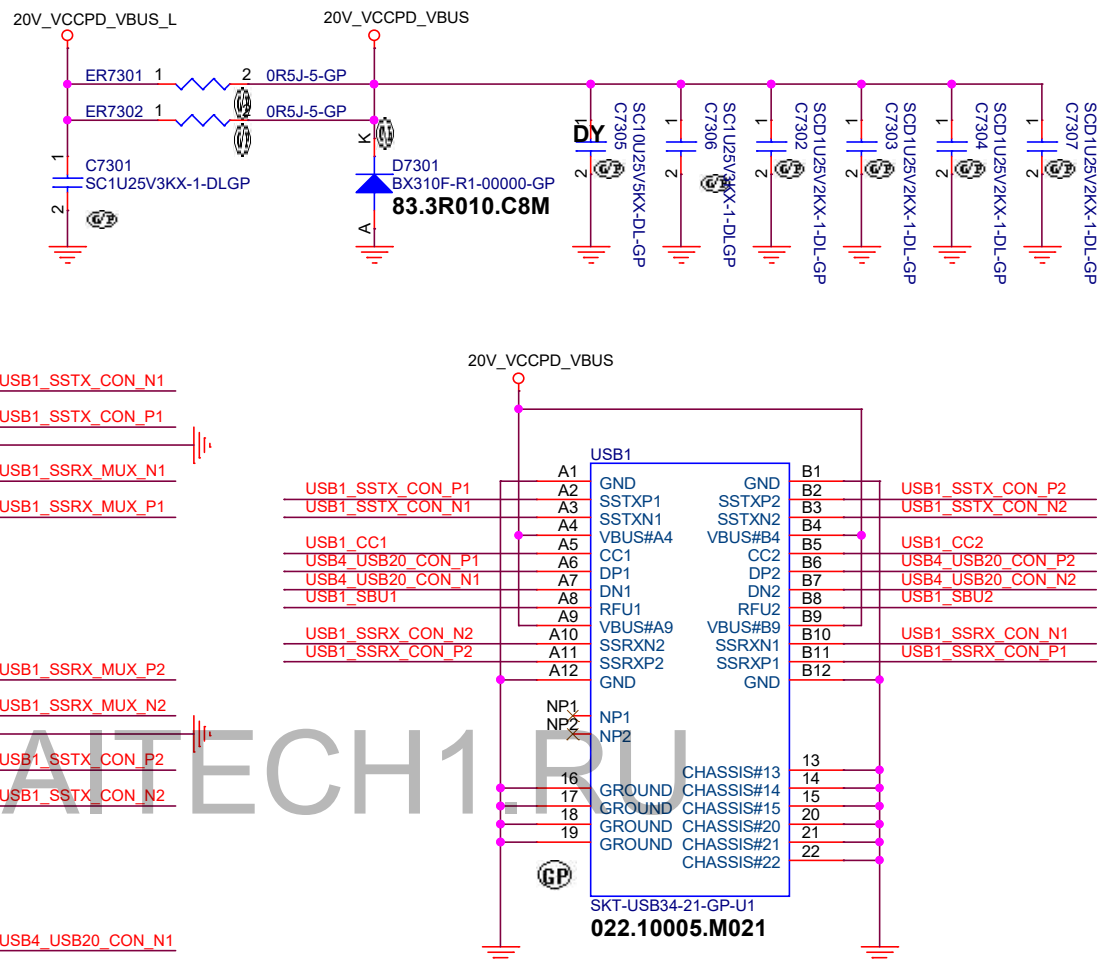
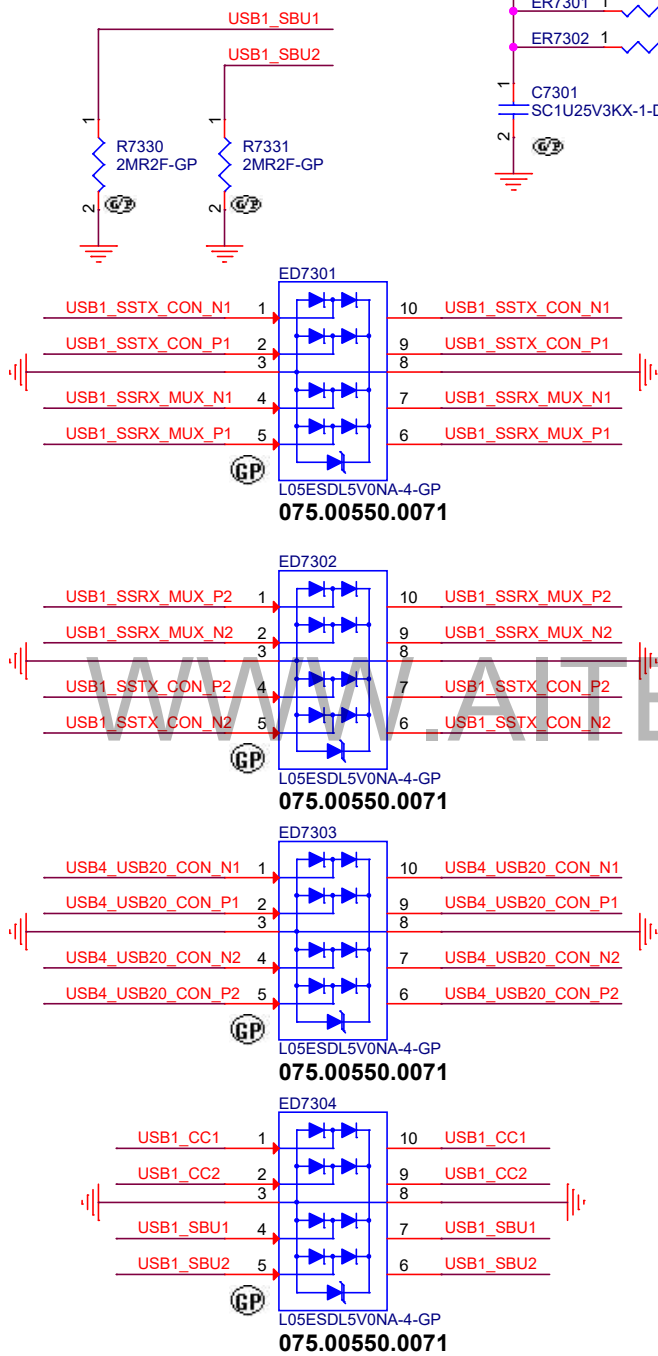
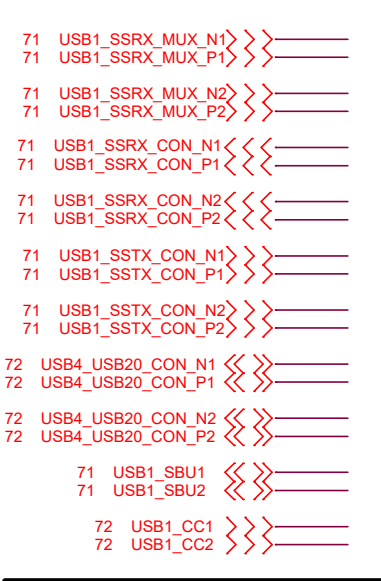
Title: **USB3.0 PORT**

Doc Number: **WASP 13" WHL-U**

Rev: **A00**

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**Main Func = TYPEC CONNECTOR**



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title	Author	Year	Source
1. The Role of the Teacher in the 21st Century	John Hattie	2009	Visible Learning
2. The Science of Learning: How the Brain Builds Knowledge	Barak A. Shiffrin	2001	Psychological Review
3. The Power of Learning Styles: Understanding How We Learn	David A. Kolb	1994	Journal of Management Education
4. The Impact of Technology on Education	Mark Prensky	2001	Marathon Education
5. The Art of Teaching: A Practical Guide	William G. Perry	1982	Harvard University Press
6. The Future of Education: A Vision for the 21st Century	Bill Gates	2007	Microsoft
7. The Science of Learning: How the Brain Builds Knowledge	Barak A. Shiffrin	2001	Psychological Review
8. The Power of Learning Styles: Understanding How We Learn	David A. Kolb	1994	Journal of Management Education
9. The Impact of Technology on Education	Mark Prensky	2001	Marathon Education
10. The Art of Teaching: A Practical Guide	William G. Perry	1982	Harvard University Press

## GPU(1/5)PEG

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Document Number

## WASP 13" WHL-U

Rev

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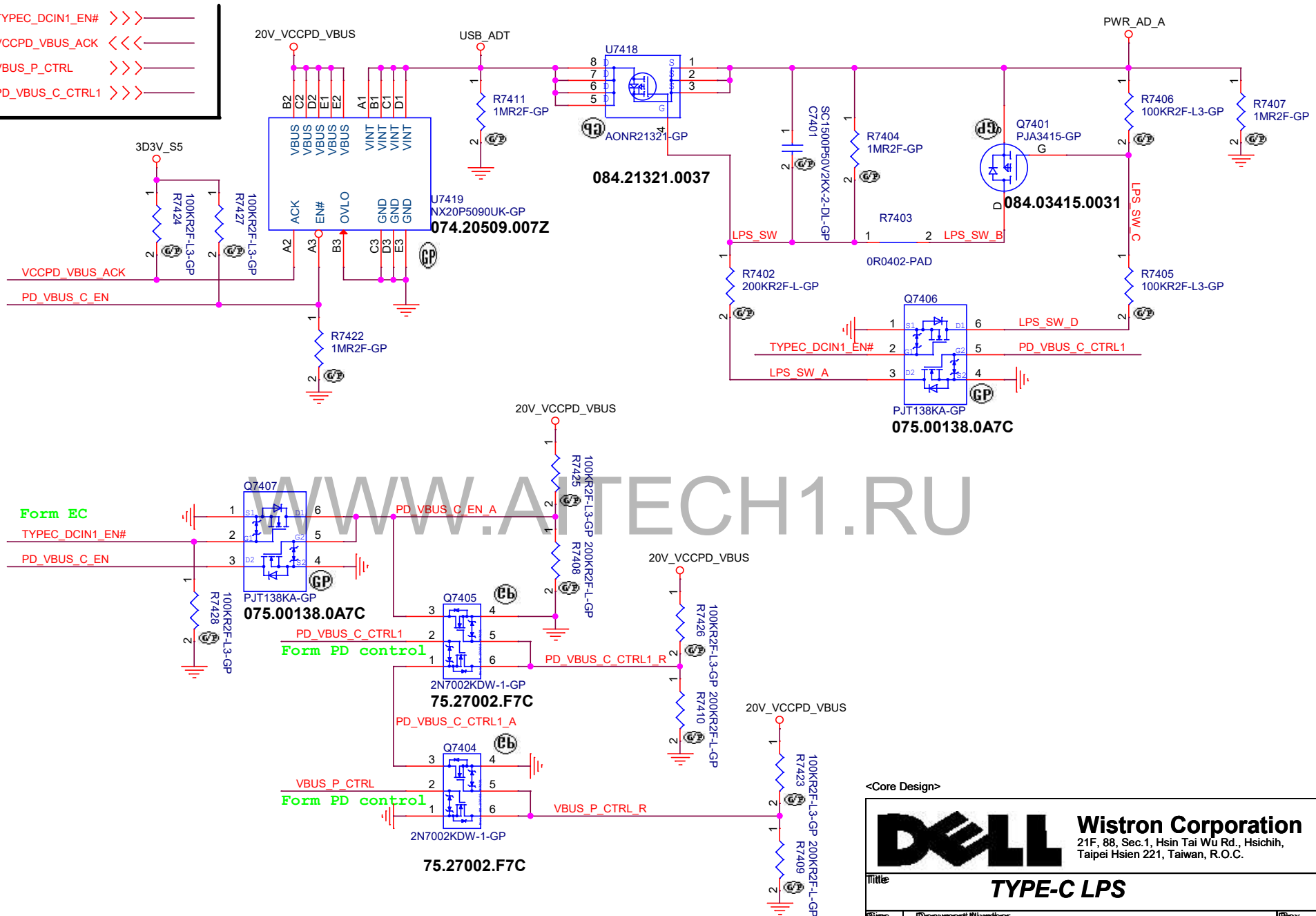
Thursday, March 07, 2019

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# Main Func = TYPEC protect

24 TYPEC\_DCIN1\_EN# >>>  
 44 VCCPD\_VBUS\_ACK <<<  
 72 VBUS\_P\_CTRL >>>  
 72 PD\_VBUS\_C\_CTRL1 >>>



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Title			<b>TYPE-C LPS</b>	
Size	Document Number		Rev	
A4			<b>WASP 13" WHL-U</b>	
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Title

**GPU(3/5)VRAM/F**

Size  
A4

Document Number

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Rev

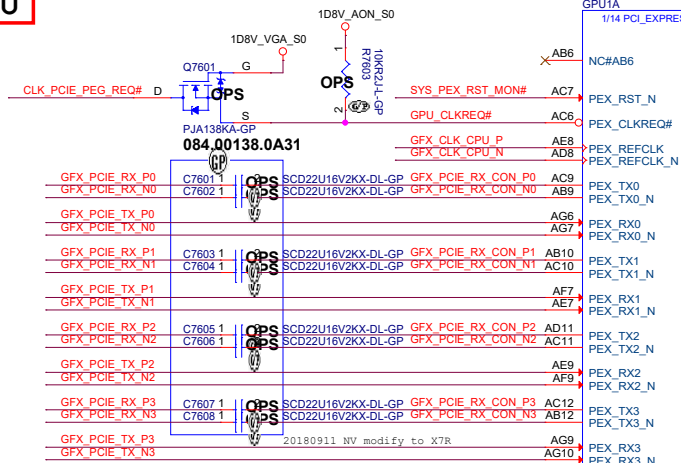
**A00**

Date: Thursday, March 07, 2019

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# Main Func = dGPU

16 GFX\_PCIE\_RX\_P0 <<<<  
16 GFX\_PCIE\_RX\_N0 <<<<  
16 GFX\_PCIE\_TX\_P0 <<<<  
16 GFX\_PCIE\_TX\_N0 <<<<  
16 GFX\_PCIE\_RX\_P1 <<<<  
16 GFX\_PCIE\_RX\_N1 <<<<  
16 GFX\_PCIE\_TX\_P1 <<<<  
16 GFX\_PCIE\_TX\_N1 <<<<  
16 GFX\_PCIE\_RX\_P2 <<<<  
16 GFX\_PCIE\_RX\_N2 <<<<  
16 GFX\_PCIE\_TX\_P2 <<<<  
16 GFX\_PCIE\_TX\_N2 <<<<  
16 GFX\_PCIE\_RX\_P3 <<<<  
16 GFX\_PCIE\_RX\_N3 <<<<  
16 GFX\_PCIE\_TX\_P3 <<<<  
16 GFX\_PCIE\_TX\_N3 <<<<  
18 CLK\_PCIE\_PEG\_REQ# <<<<  
18 GFX\_CLK\_CPU\_P <<<<  
18 GFX\_CLK\_CPU\_N <<<<  
85 VGACORE\_VDD\_SENSE\_1 <<<<  
85 VGACORE\_GND\_SENSE\_1 <<<<  
17.61,63,66,91 PLTRST#\_CPU >>>>  
20 DGPU\_HOLD\_RST# >>>>



Remove the GPIO16/21 connection for GC6 2.1 to saving the layout spacing.

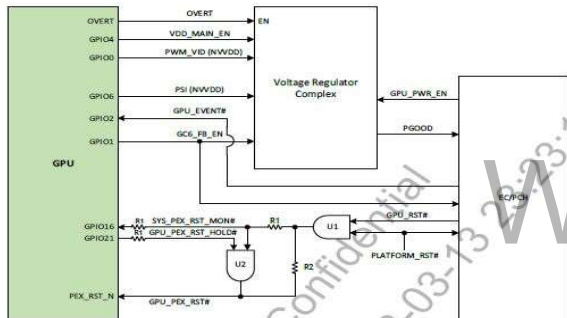


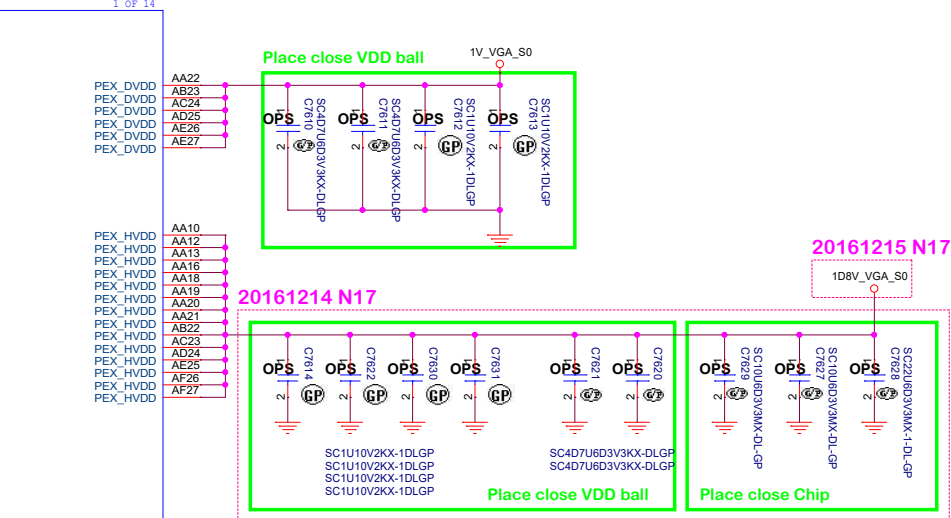
Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	N16	N17	Location
<b>N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail</b>						
GB2B-64, GB2C-64	1.0 $\mu$ F	X65 0402	1	1		Under GPU
	4.7 $\mu$ F	X65 0603	0	1		Under GPU
	4.7 $\mu$ F	X65 0603	1	2		Near GPU
	10 $\mu$ F	X65 0805	0	2		Midway between GPU and Power Supply
	22 $\mu$ F	X65 0805	0	1		Midway between GPU and Power Supply
<b>N16 PEX_IOVDD (N17 PEX_HVDD) Supply Rail</b>						
GB2B-64, GB2C-64	1.0 $\mu$ F	X65 0402	1	4		Under GPU
	4.7 $\mu$ F	X65 0603	1	2		Near GPU
	10 $\mu$ F	X65 0805LP	1	2		Midway between GPU and Power Supply
	22 $\mu$ F	X65 0805LP	1	1		Midway between GPU and Power Supply

NC FOR GM108



NC FOR GF119

PEX\_PLL\_HVDD

PEX\_PLL\_HVDD

NC#A8B

20180907 Remove TP

AF22

AE22

NC#AA14

NC#AA15

20180907 Remove TP

AF24

AE24

AF21

AE21

AG24

AG25

AG21

AG22

AF25

PEX\_TERM

2K49R2F-GP

071.0N17S.0000

17S-G1-X1-GP

071.0N17S.0000

17S-G1-X1-GP

071.0N17S.0000

17S-G1-X1-GP

071.0N17S.0000

17S-G1-X1-GP

071.0N17S.0000

17S-G1-X1-GP

071.0N17S.0000

GPU	Capacitor Type	Footprint	Population	N16	N17	Location
<b>PEX_PLL_HVDD Supply Rail</b>						
GB2B-64, GB2C-64	0.1 $\mu$ F	X7R 0402	1	1		Near GPU

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Title: **GPU(1/5)PEG**

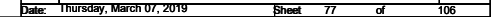
Site Custom: **WASP 13" WHL-U**

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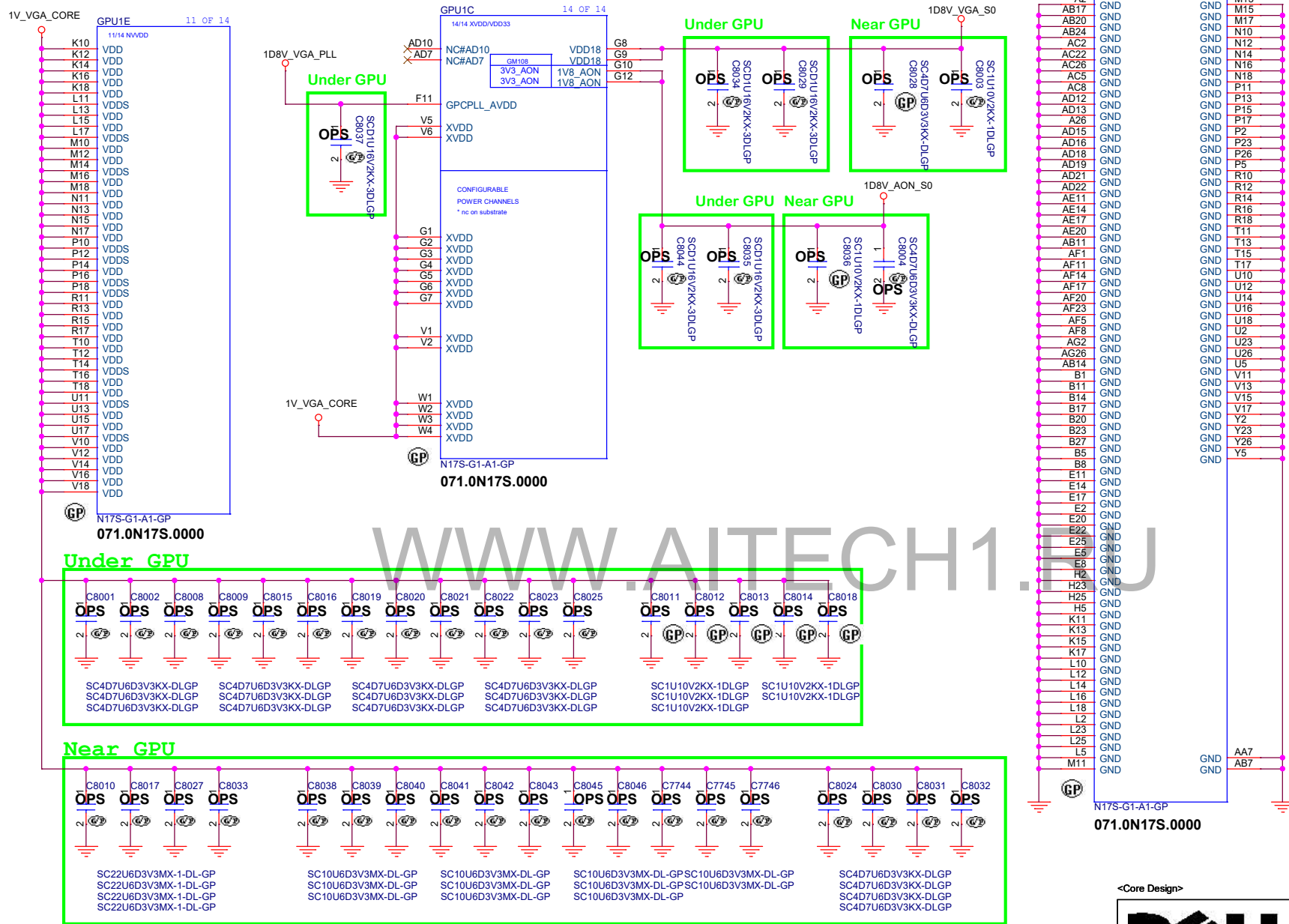
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## Main Func = dGPU



## <Core Design>



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**GPU(5/5)PWR/GND**

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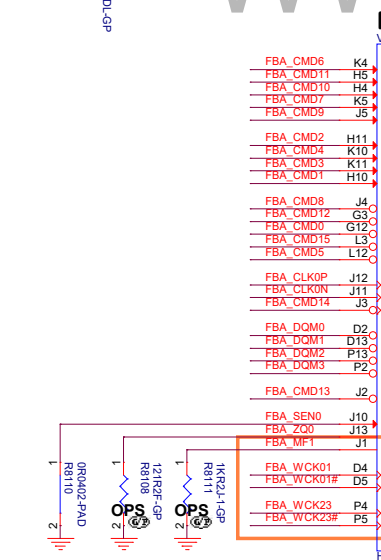
Rev  
**A00**

Date: Thursday, March 07, 2019

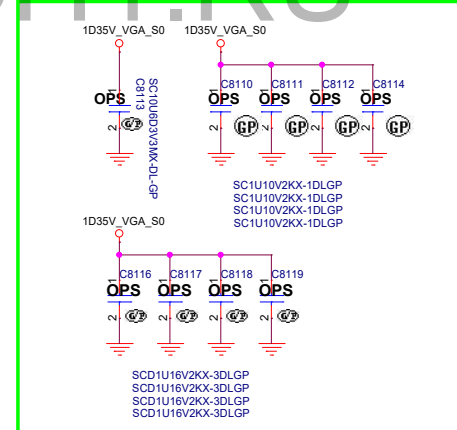
Sheet	80
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06

78,81 FBA\_CMD13 >>>\_\_\_\_\_



Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

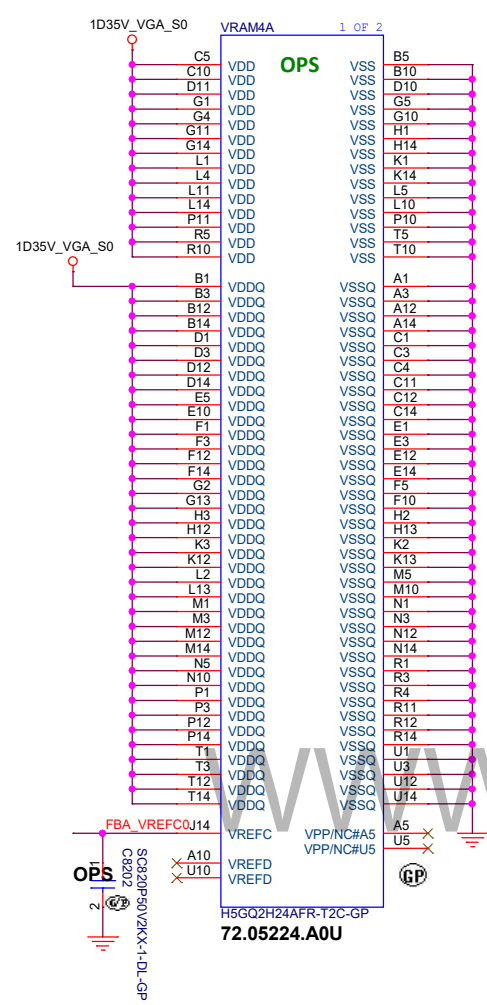


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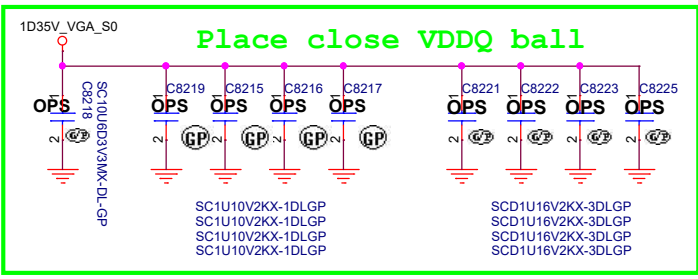
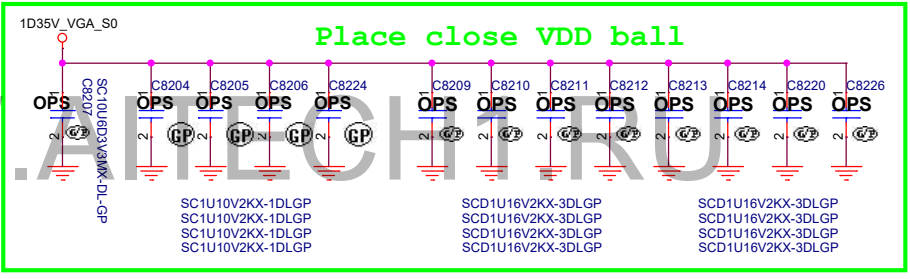
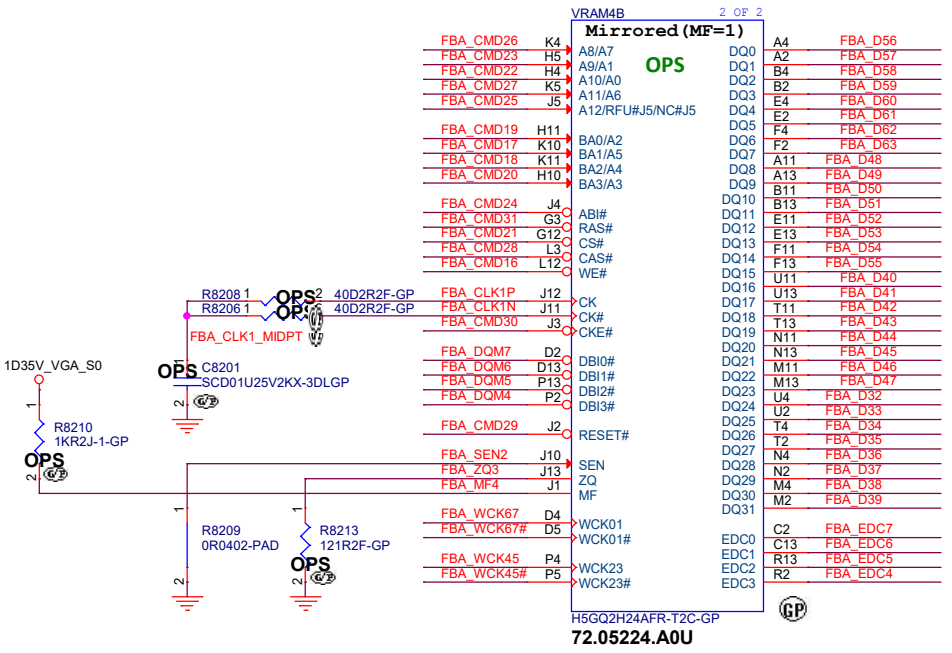
# SSID = VRAM

- 78 FBA\_D[32..63] <<<>>>
- 78 FBA\_CMD16 <<<>>>  
78 FBA\_CMD17 <<<>>>  
78 FBA\_CMD18 <<<>>>  
78 FBA\_CMD19 <<<>>>  
78 FBA\_CMD20 <<<>>>  
78 FBA\_CMD21 <<<>>>  
78 FBA\_CMD22 <<<>>>  
78 FBA\_CMD23 <<<>>>  
78 FBA\_CMD24 <<<>>>  
78 FBA\_CMD25 <<<>>>  
78 FBA\_CMD26 <<<>>>  
78 FBA\_CMD27 <<<>>>  
78 FBA\_CMD28 <<<>>>  
78 FBA\_CMD29 <<<>>>  
78 FBA\_CMD30 <<<>>>  
78 FBA\_CMD31 <<<>>>
- 78 FBA\_WCK67 <<<>>>  
78 FBA\_WCK67# <<<>>>  
78 FBA\_WCK45 <<<>>>  
78 FBA\_WCK45# <<<>>>
- 78 FBA\_DQM4 <<<>>>  
78 FBA\_DQM5 <<<>>>  
78 FBA\_DQM6 <<<>>>  
78 FBA\_DQM7 <<<>>>
- 78 FBA\_EDC4 <<<>>>  
78 FBA\_EDC5 <<<>>>  
78 FBA\_EDC6 <<<>>>  
78 FBA\_EDC7 <<<>>>
- 78 FBA\_CLK1P <<<>>>  
78 FBA\_CLK1N <<<>>>
- 81 FBA\_VREFC0 <<<>>>
- 79.81 GPIO10\_FBVREF <<<>>>




FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



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Title

GPU-VRAM3,4 (2/4)

Size

Custom

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>GPU-VRAM5,6 (3/4)</b>		
Size A4	Document Number <b>WASP 13" WHL-U</b>	Rev <b>A00</b>
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<Core Design>

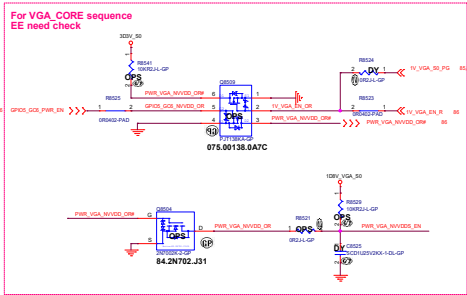
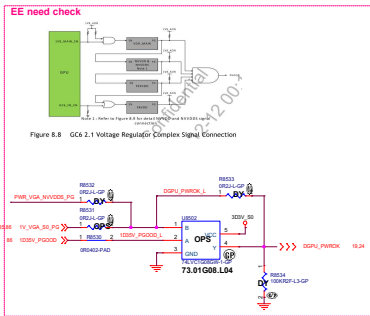
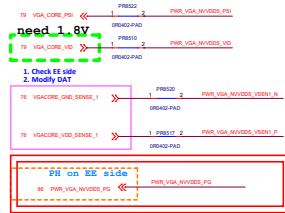


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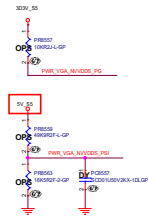
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Size	Document Number		Rev
A4	<b>WASP 13" WHL-U</b>		<b>A00</b>
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# OFFPAGE-Signal



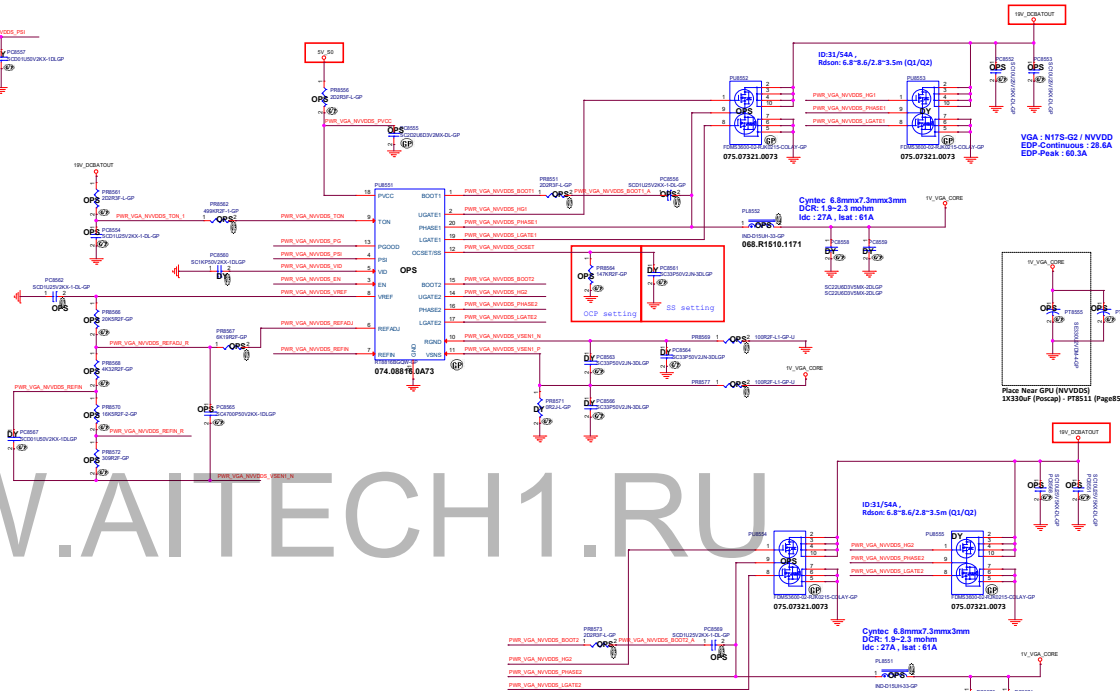
# OFFPAGE-GAP



# RT8816A For NVVDDS

VGA : N175-G2 / NVVDD  
EDP-Continuous : 28.6A  
EDP-Peak : 60.3A

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.00V to 1.35V
2phase with CCM	1.8V to 5.5V



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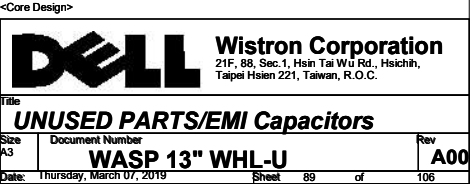
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## Main Func = UnusedParts



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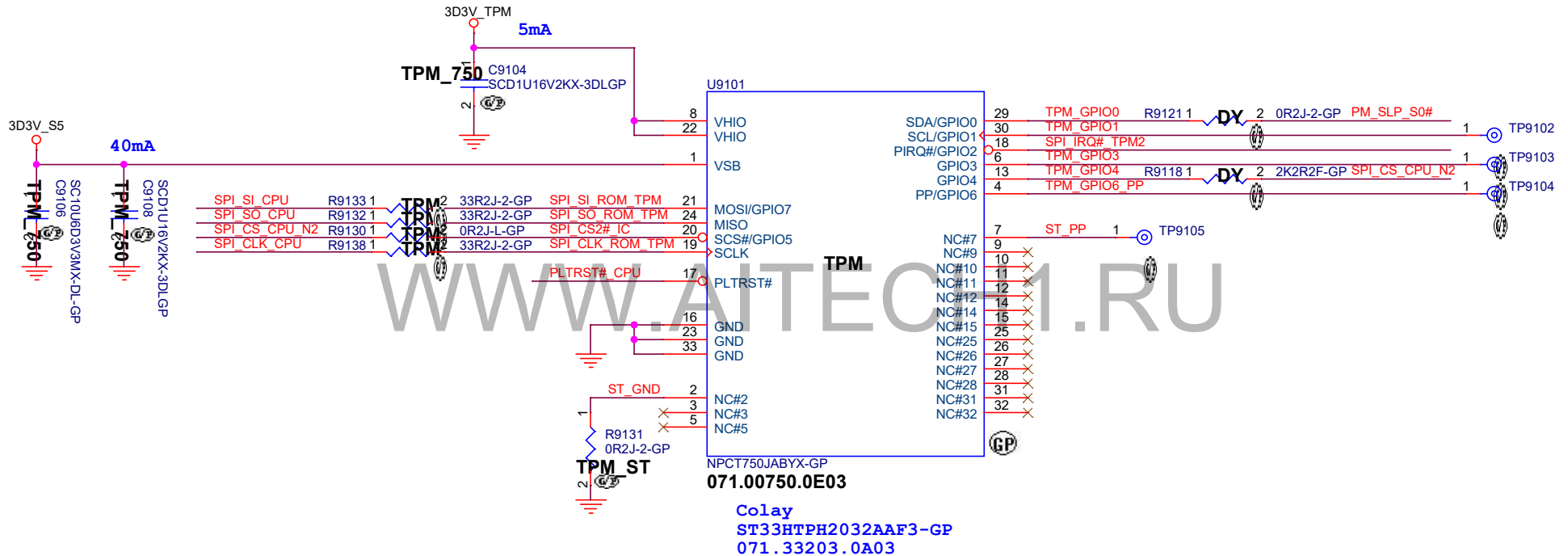
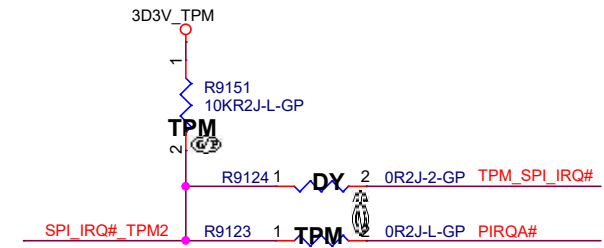
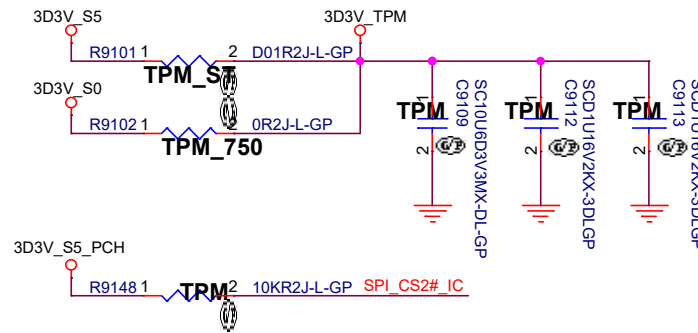
**A00**

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# Main Func = TPM

15,18,25 SPI\_SI\_CPU >>>—  
 18 SPI\_CS\_CPU\_N2 >>>—  
 18,25 SPI\_CLK\_CPU >>>—  
 18,25 SPI\_SO\_CPU <<<—  
 17,40 PM\_SLP\_S0# >>>—  
 17,61,63,66,76 PLTRST#\_CPU >>>—  
 18 TPM\_SPI\_IRQ# >>>—  
 20 PIRQA# >>>—



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Title			TPM2.0	
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A4	WASP 13" WHL-U		A00	
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Title

***LVDS Switch***

Size  
A4

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Rev

**A00**

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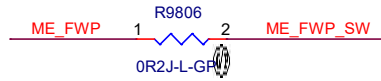
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**Main Func = SWITCH**

```

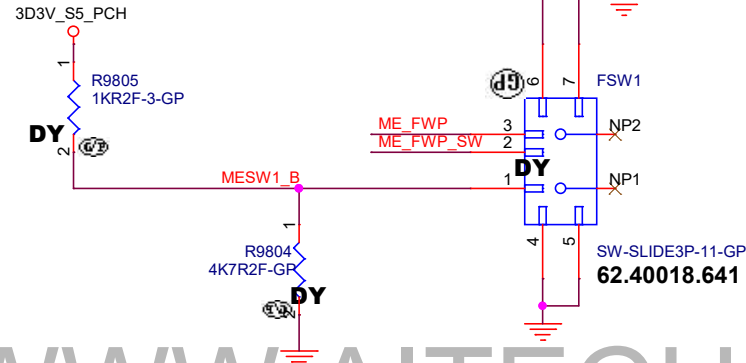
24 ME_FWP      >>>_____
19 ME_FWP_SW  <<<_____

```



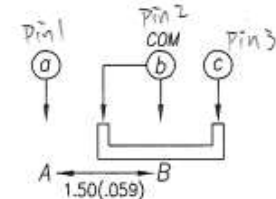
## Firmware SW

Default setting:pull LOW  
DY for MP

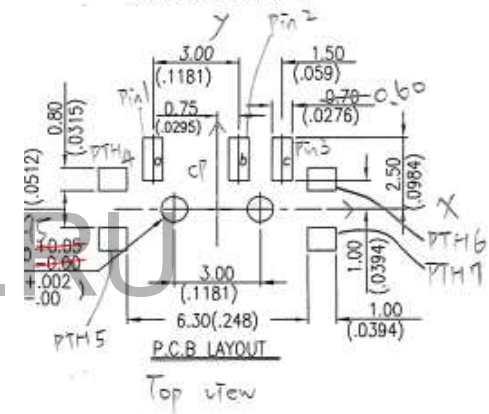


	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

\*Symbol same as.  
62,40018,461.



CIRCUIT DIAGRAM



## <Core Design>



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Title
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## **CRT Switch**

Size

Size	Document Number
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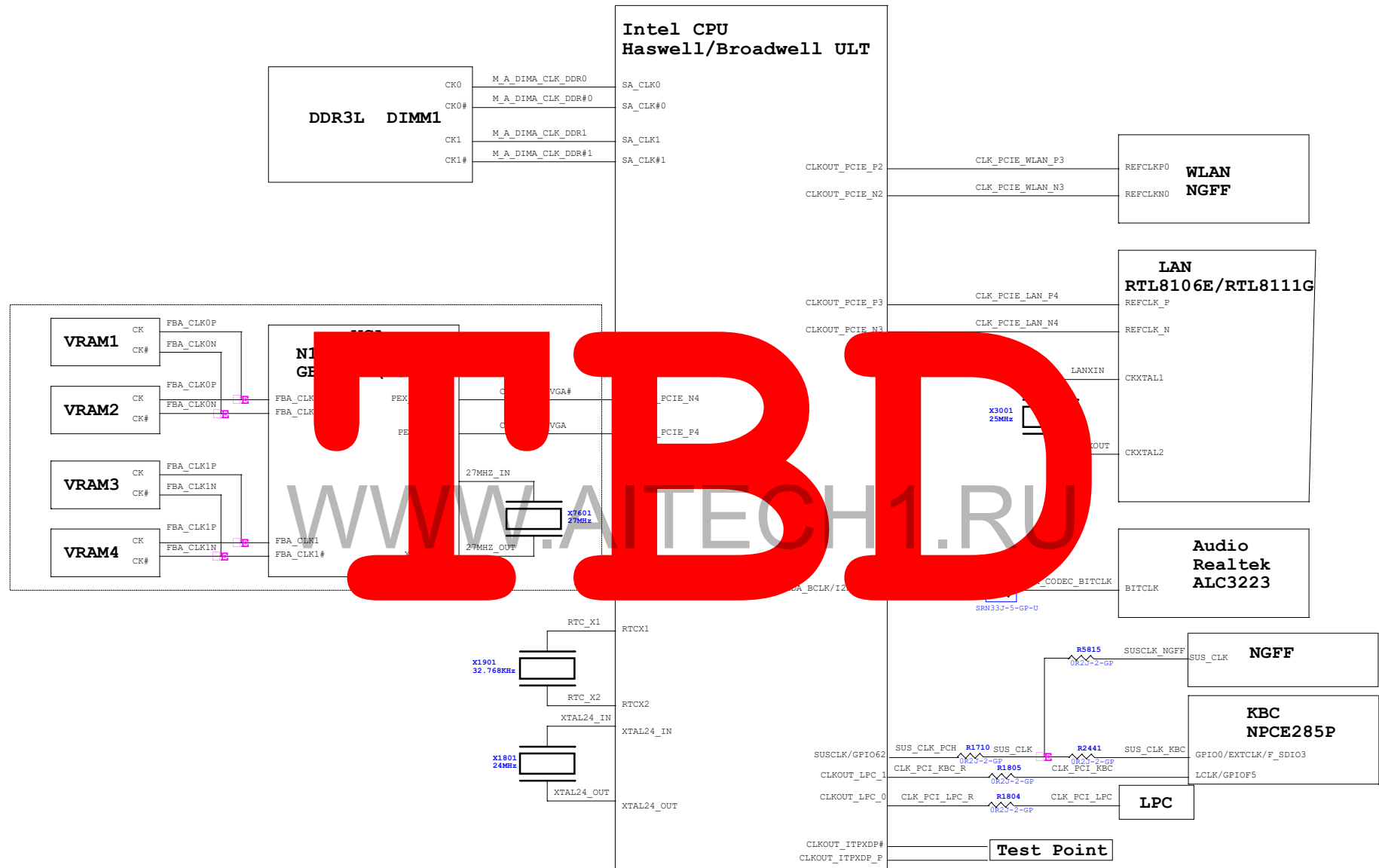
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Title					
CPU XDP;PCH XDP					
Size A4	Document Number				Rev
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# CLK Block Diagram





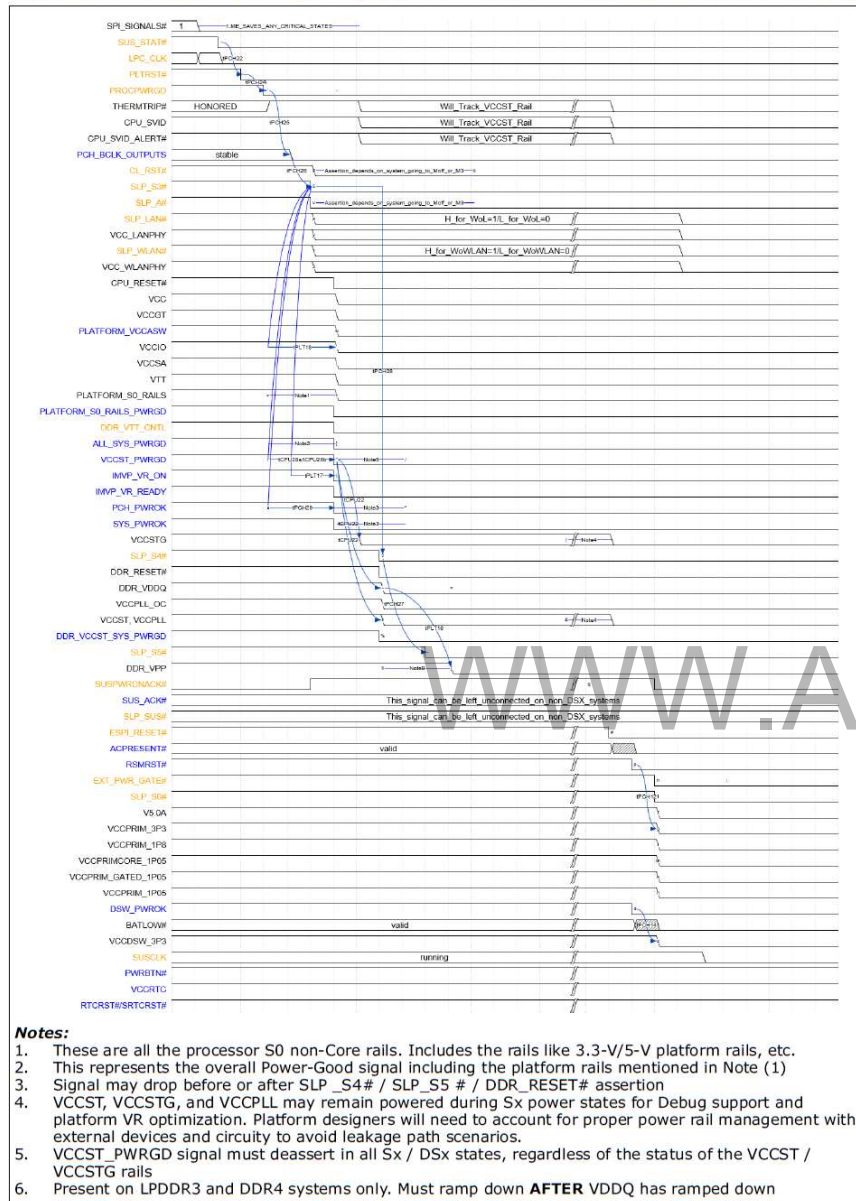
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Figure 12-21.WHL-U Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]



<Core Design>



Power Sequence		
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